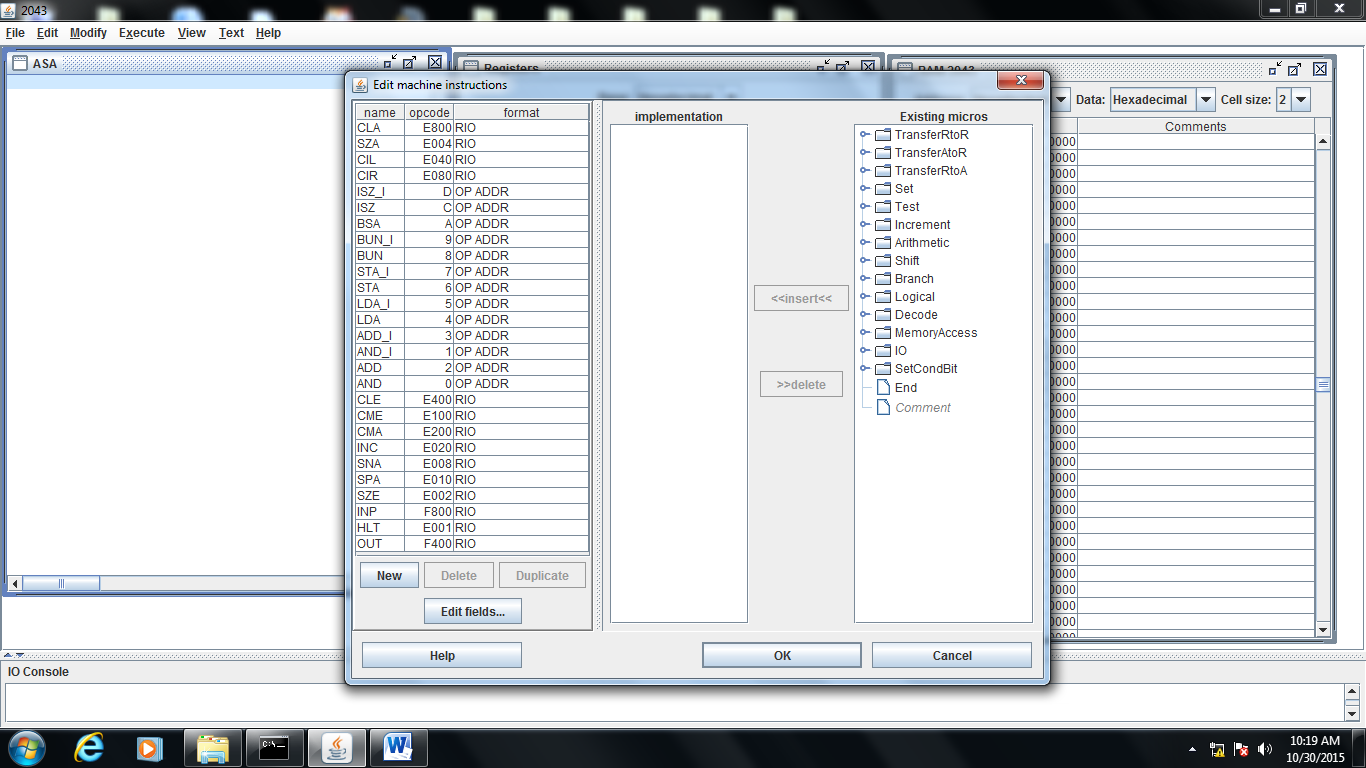
# CSA ASSIGNMENT

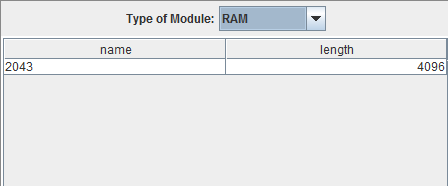
**Name- Pranav Gurditta**

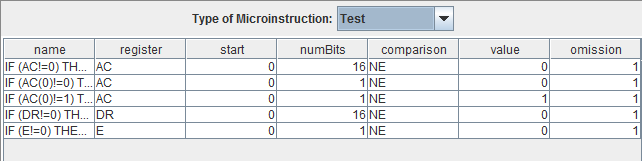
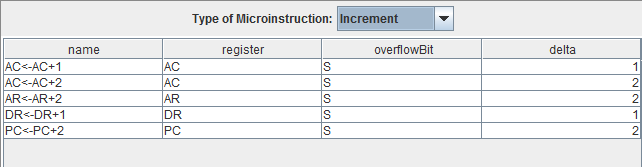
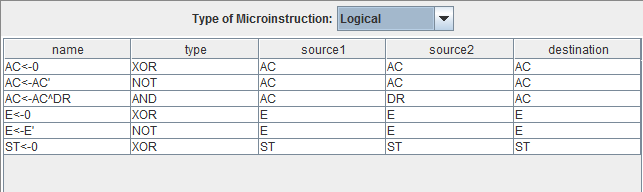
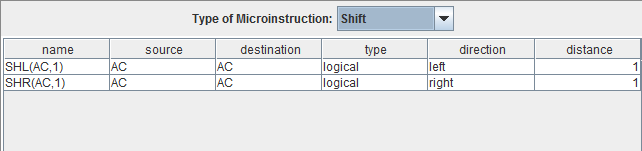
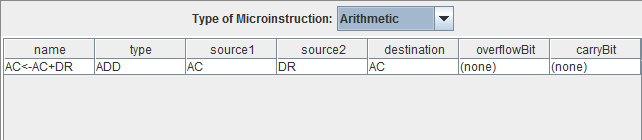
**Roll number- 2K15/CS/2002**

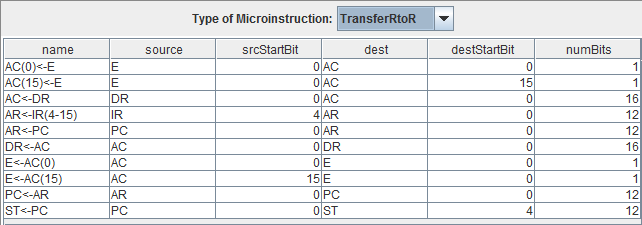
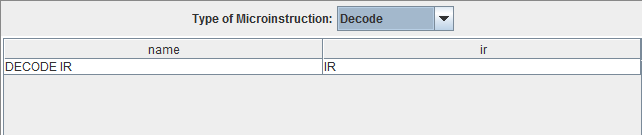
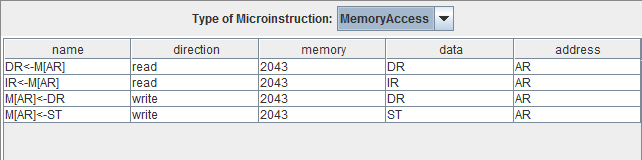
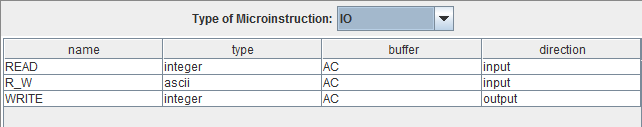
**Course- BSc. (H) Computer Science**

**Subject- Computer system architecture**

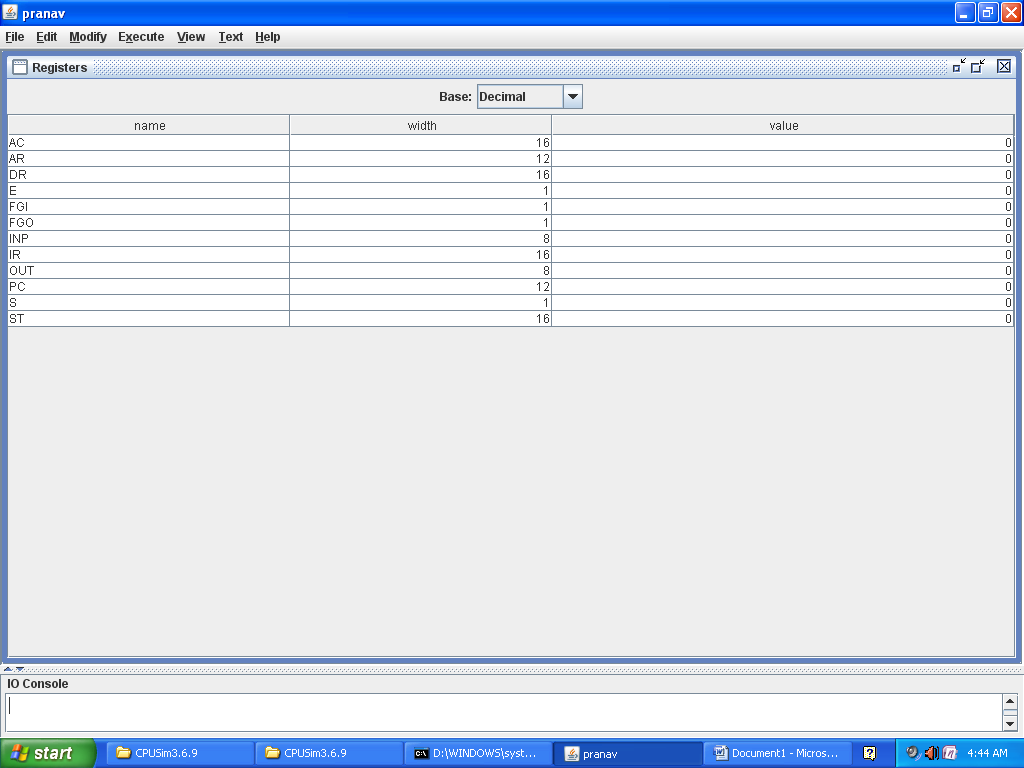




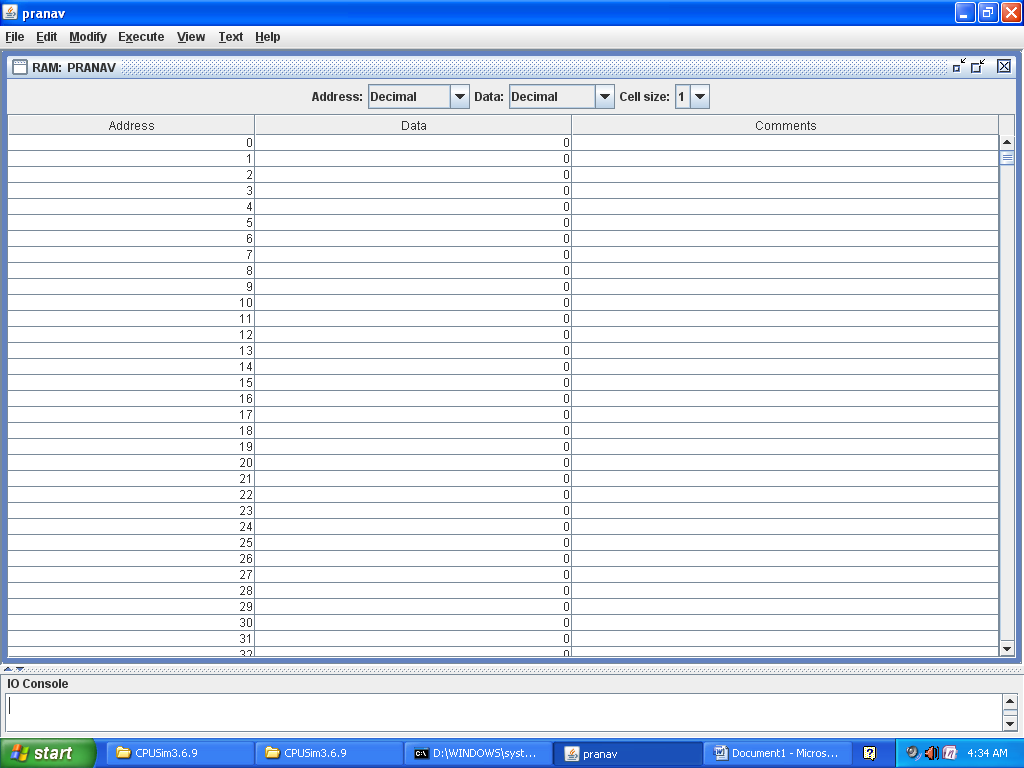
LIST OF MICRO-INSTRUCTIONS IN DIFFERENT CATEGORIES



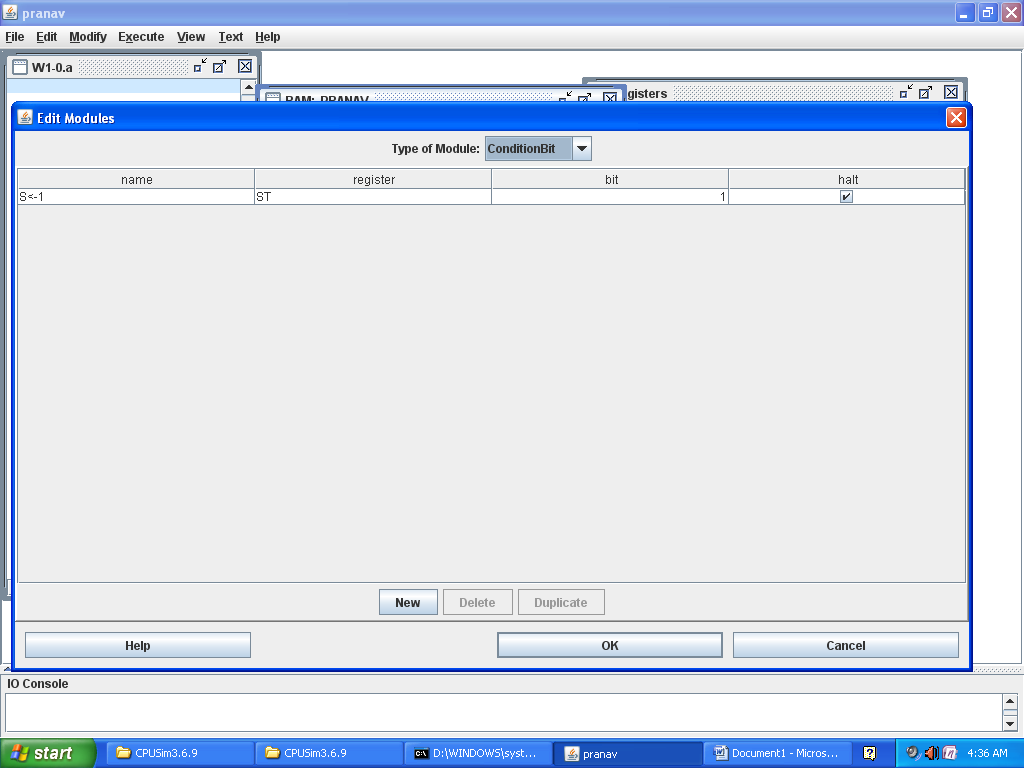
REGISTERS



RAM(MEMORY)

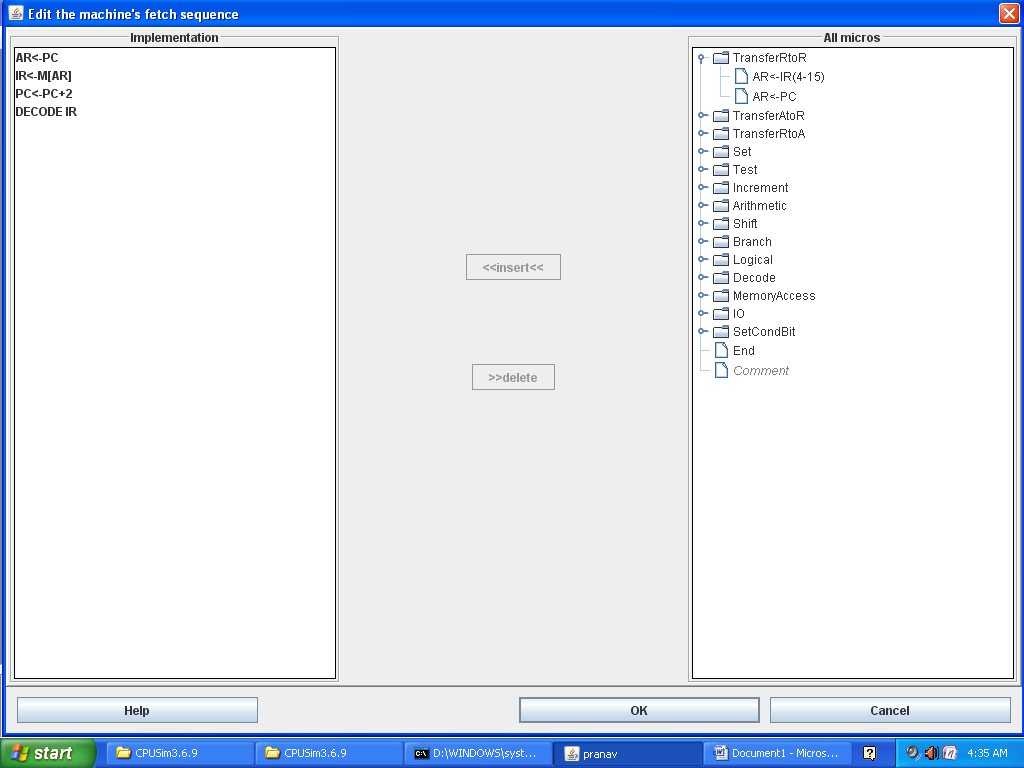


**SET CONDITION BIT**

****

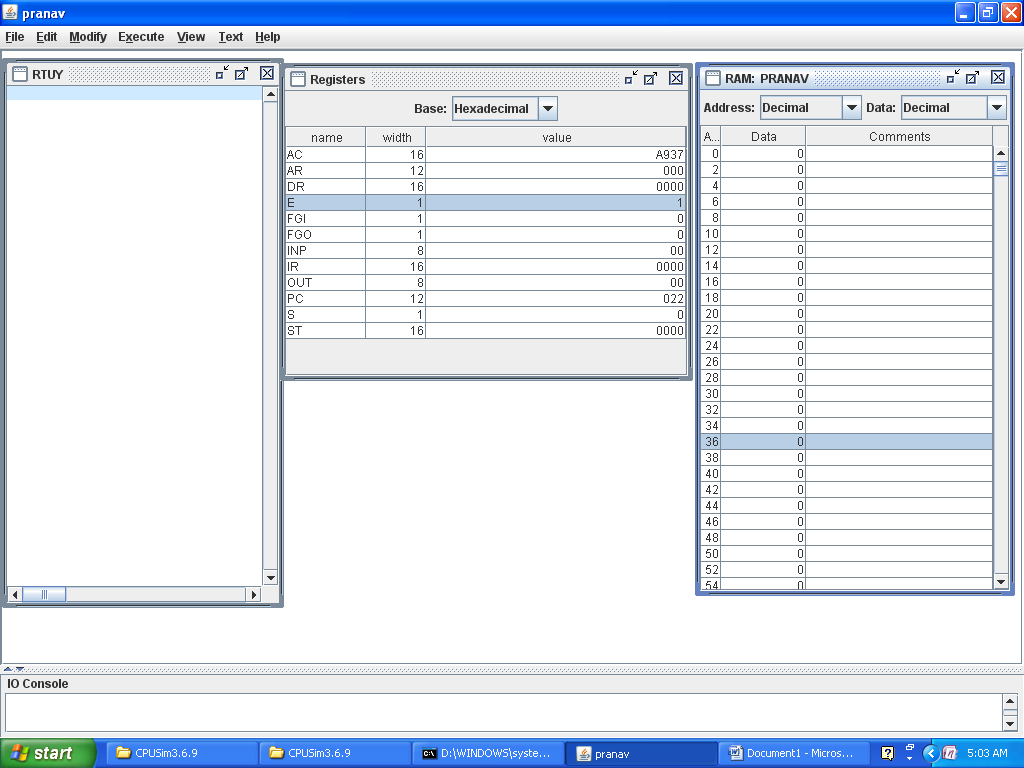
**QUESTION NO 2**

FETCH SEQUENCE

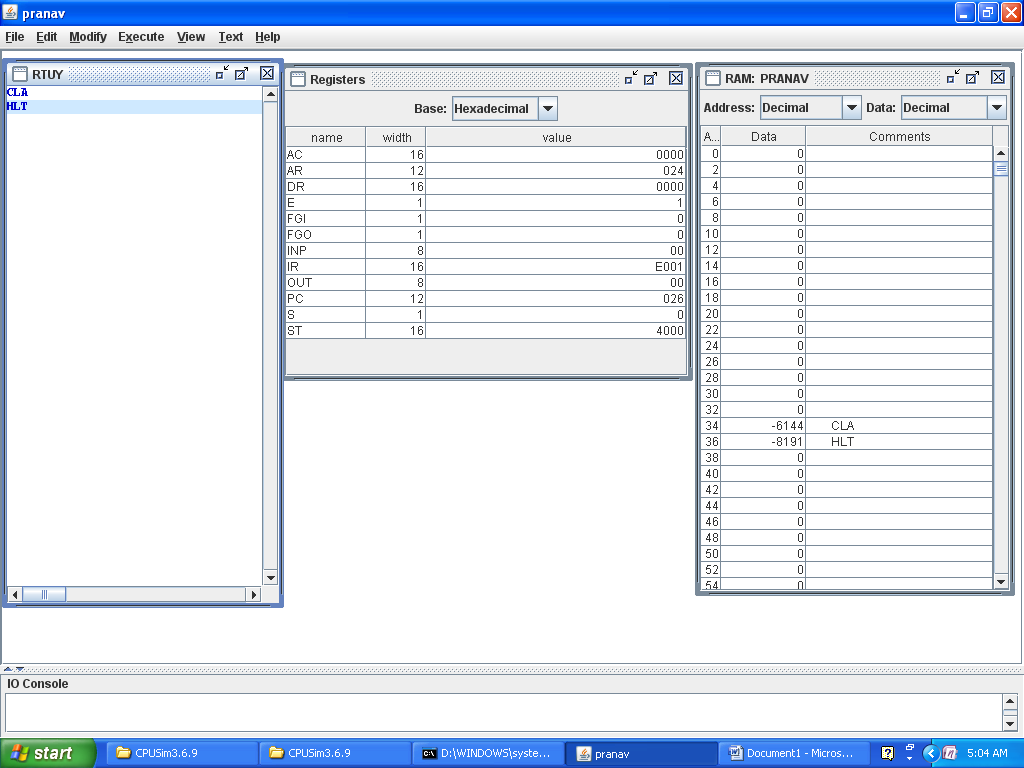


***QUESTION NO 3***

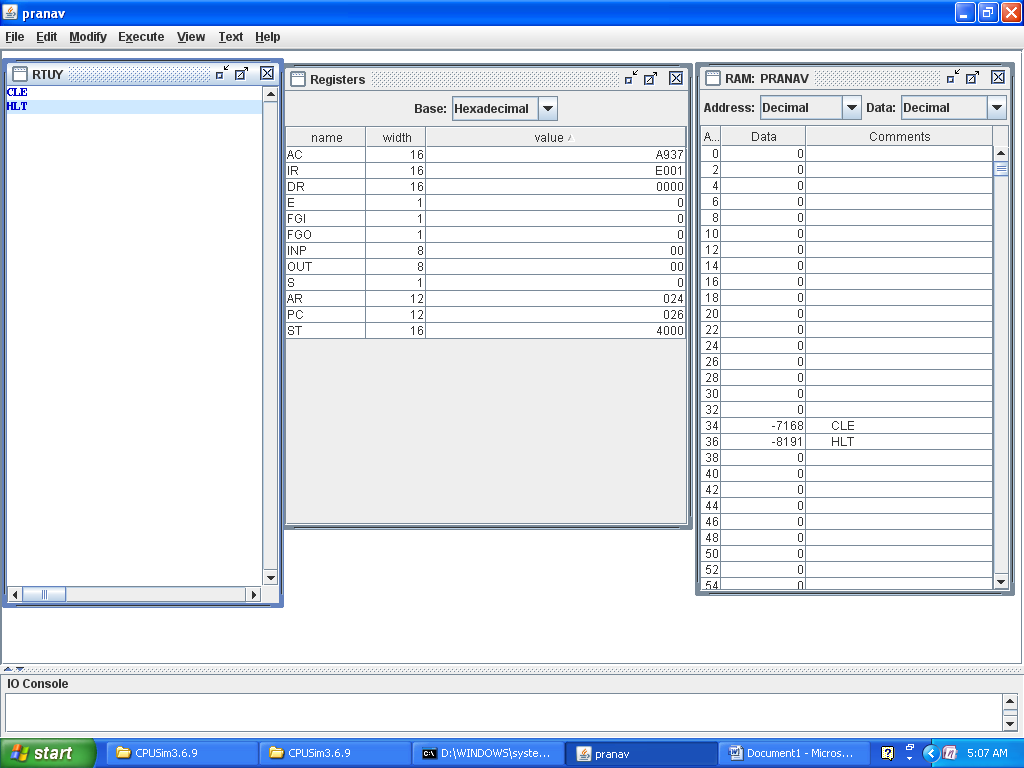
***DIRECT MACHINE***

******

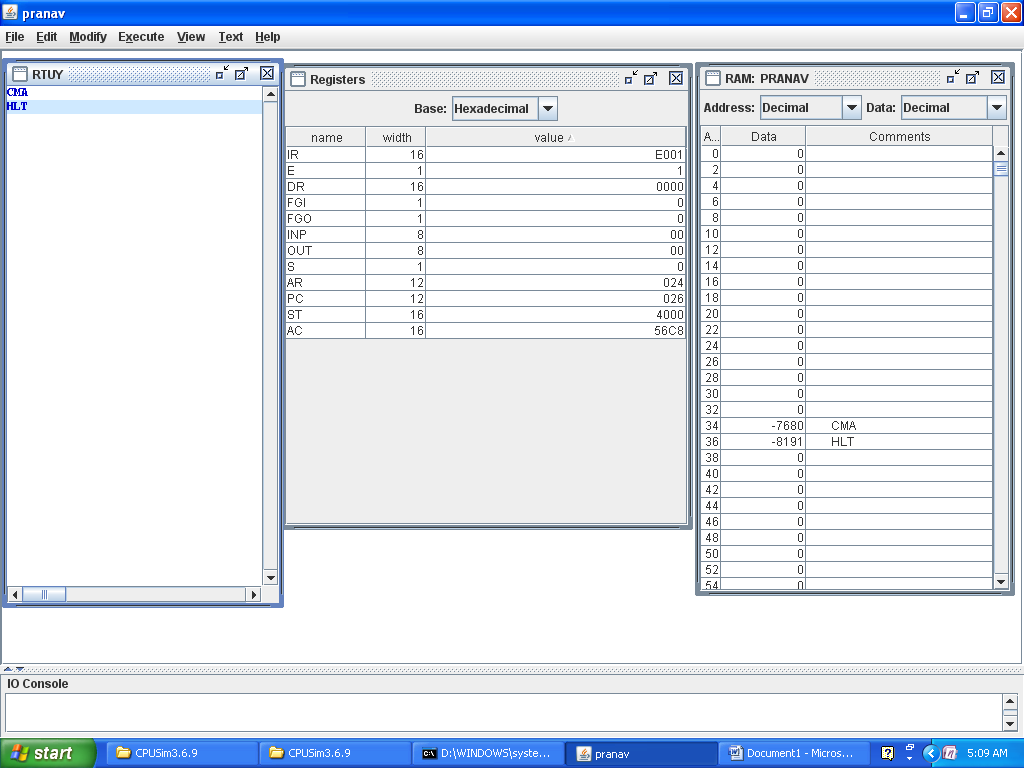
* + 1. **CLA**

****

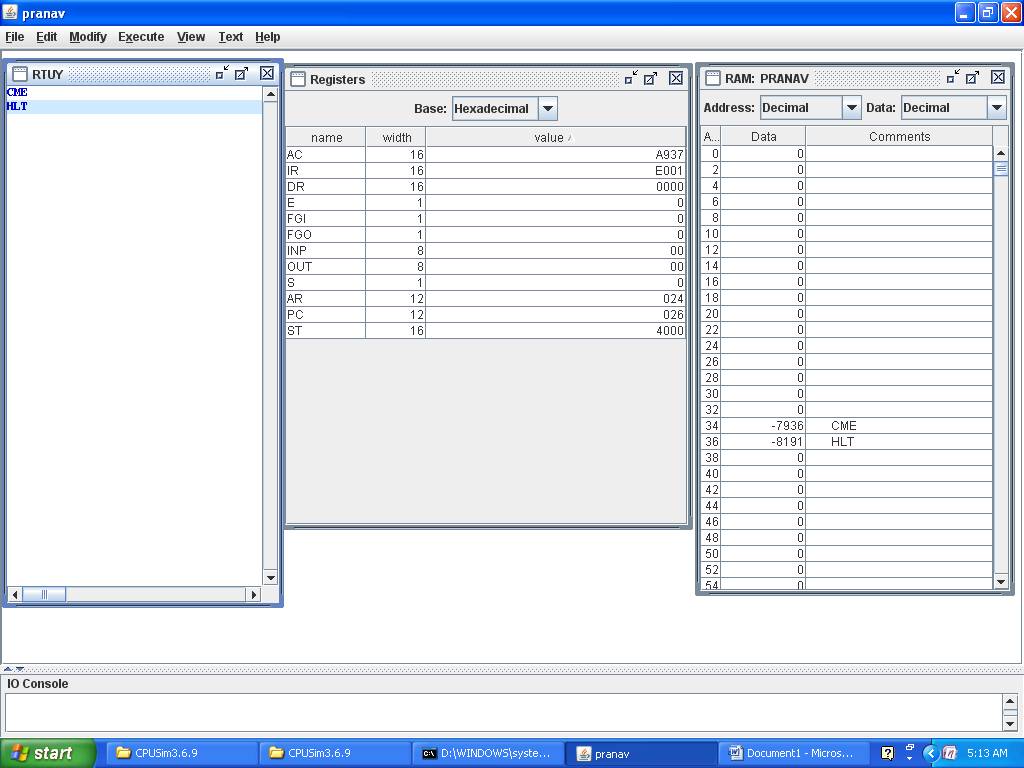
* + 1. **CLE**

****

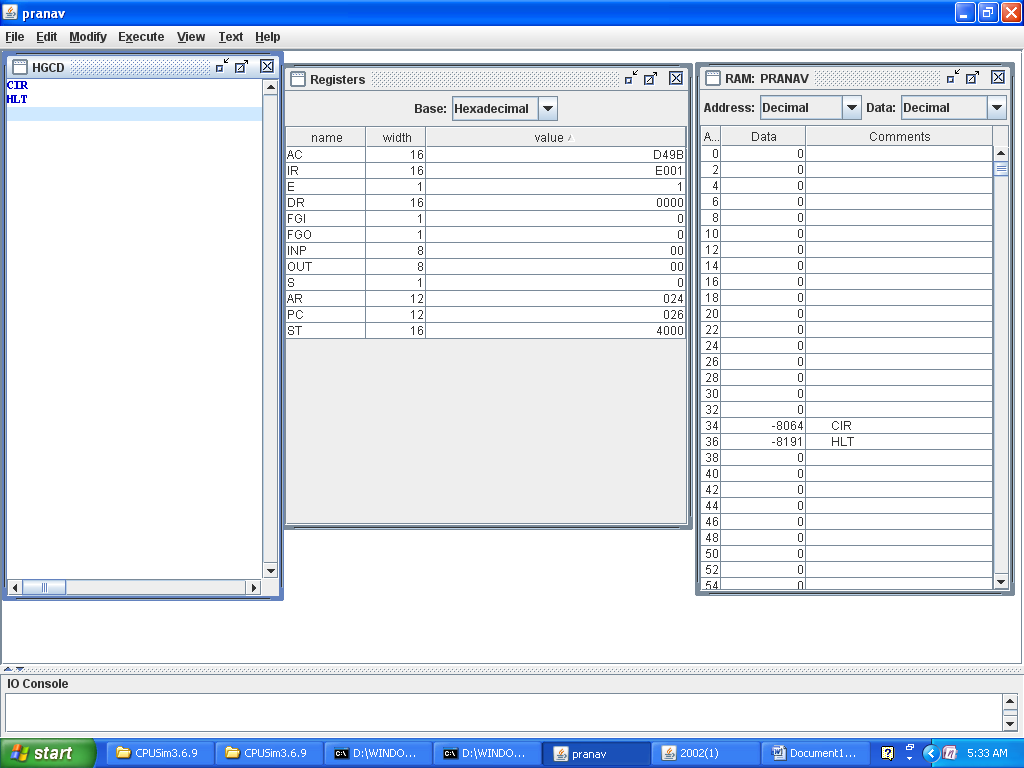
* + 1. **CMA**

****

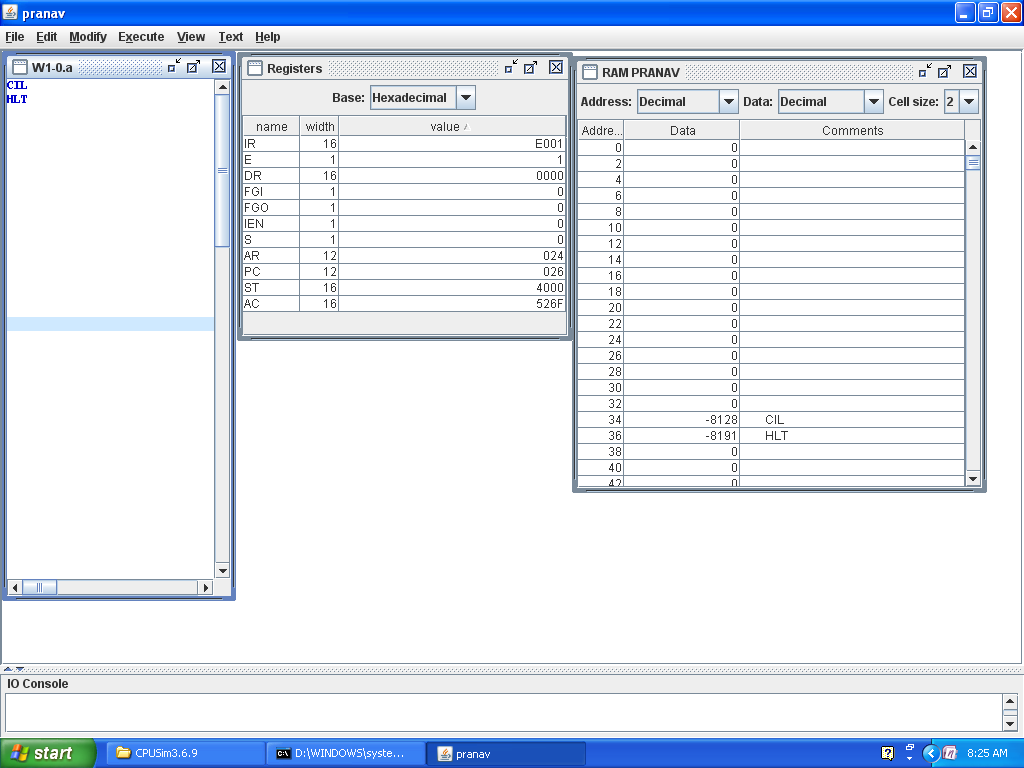
* + 1. **CME**

****

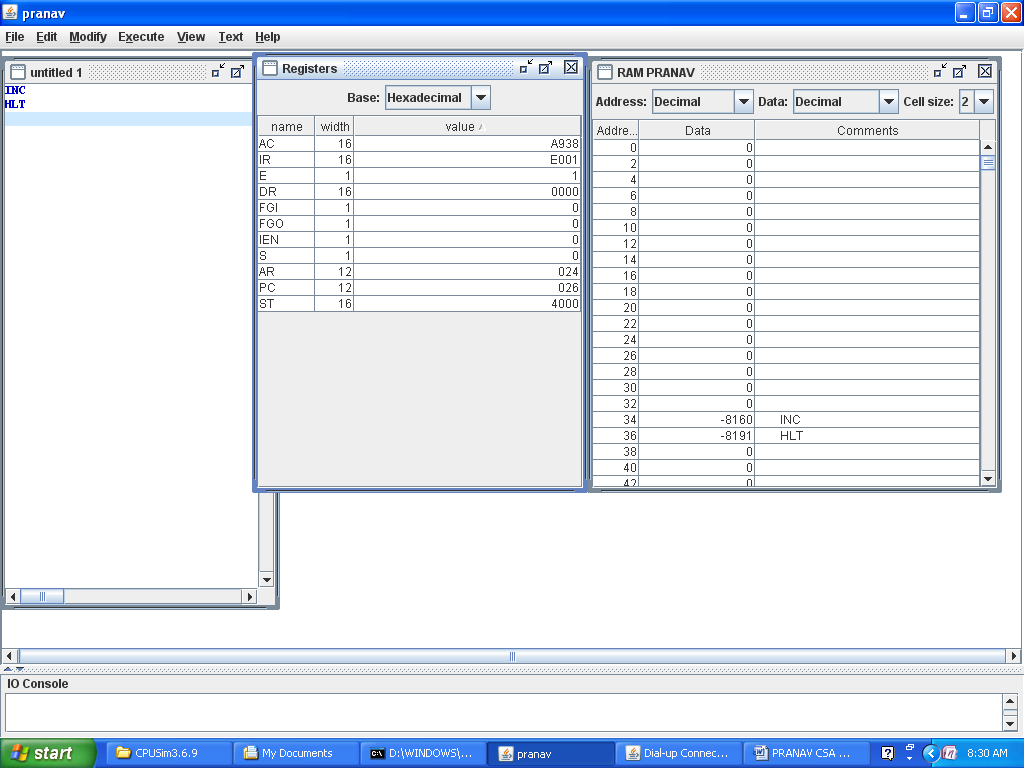
* + 1. **CIR**

****

* + 1. **CIL**

****

* + 1. **INC**

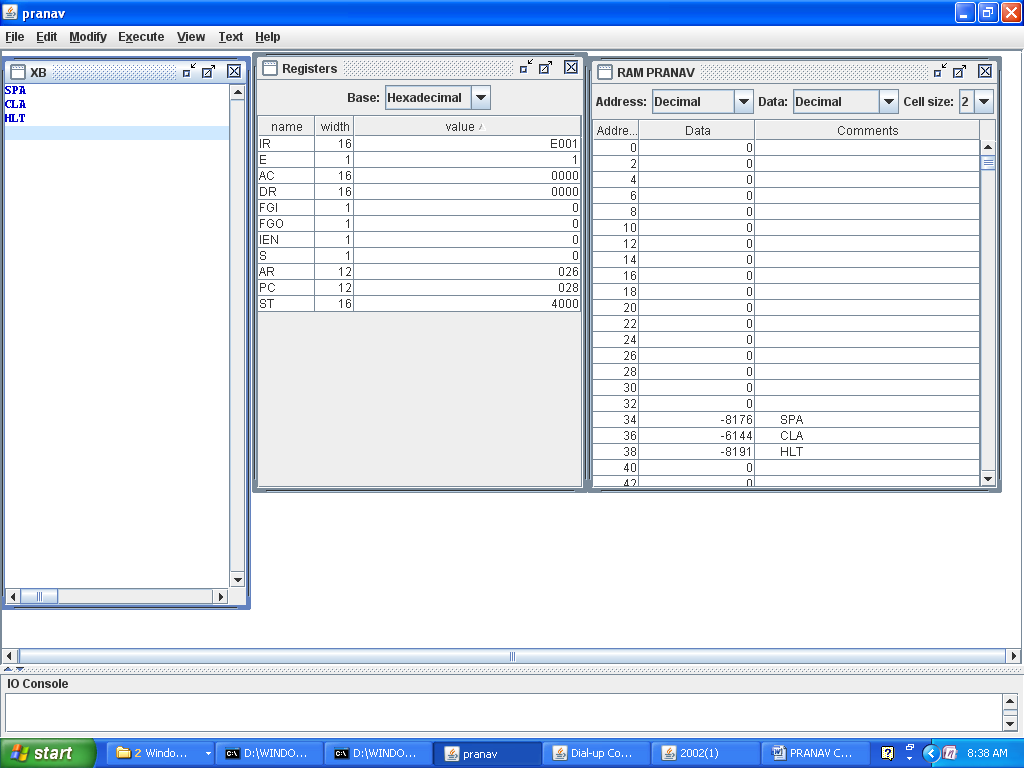
****

* + 1. **SPA**

**(SPA**

**CLA**

**HLT)**

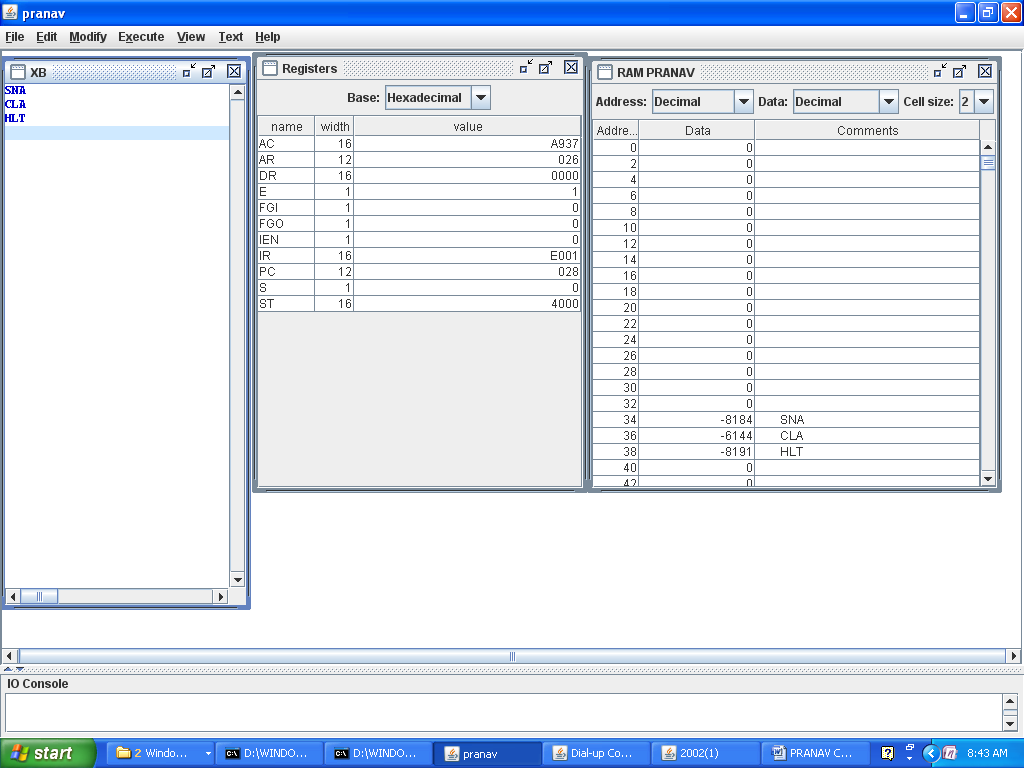
****

* + 1. **SNA**

**(SNA**

**CLA**

**HLT)**

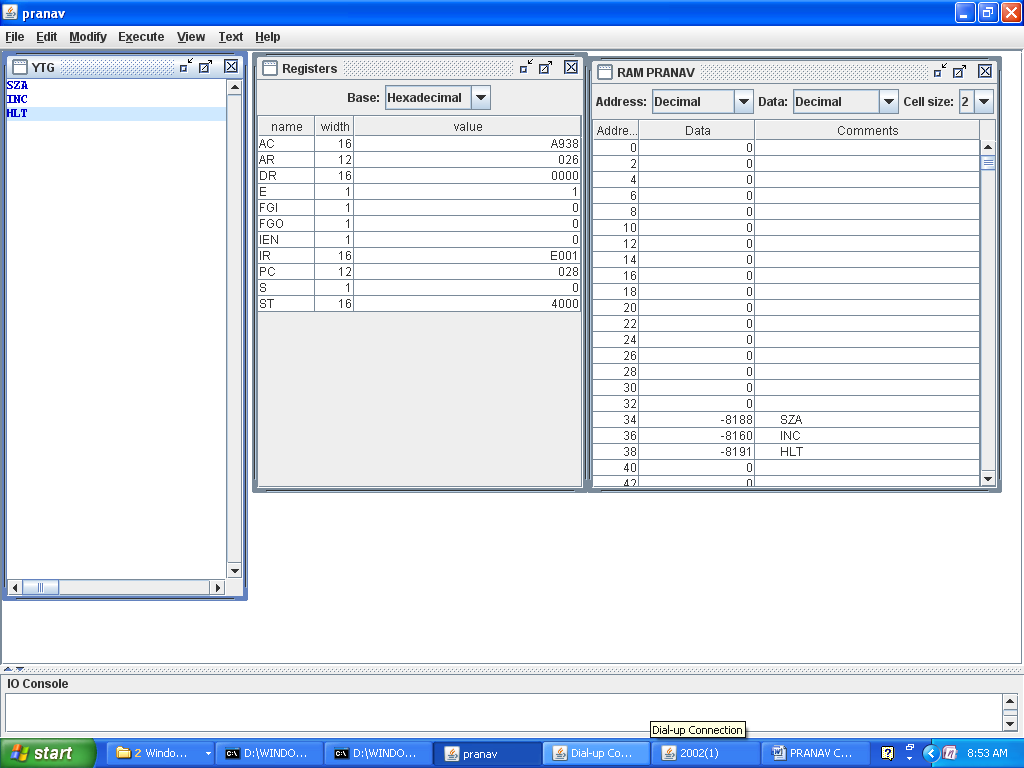
****

* + 1. **SZA**

**(SZA**

**INC**

**HLT)**

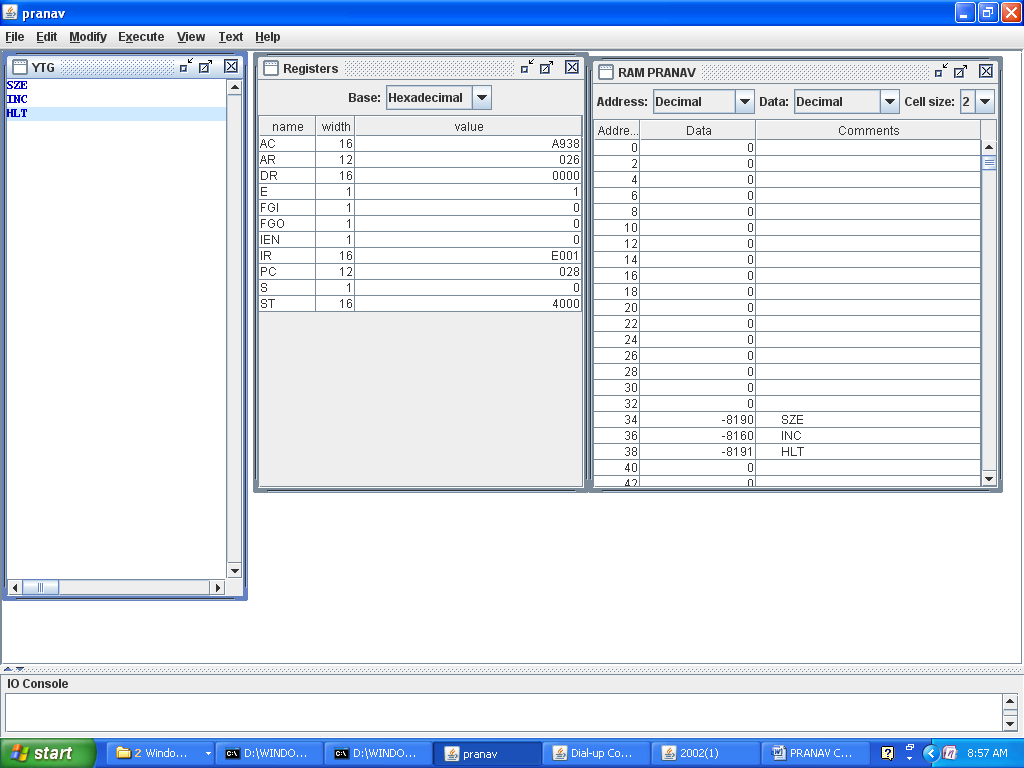
****

* + 1. **SZE**

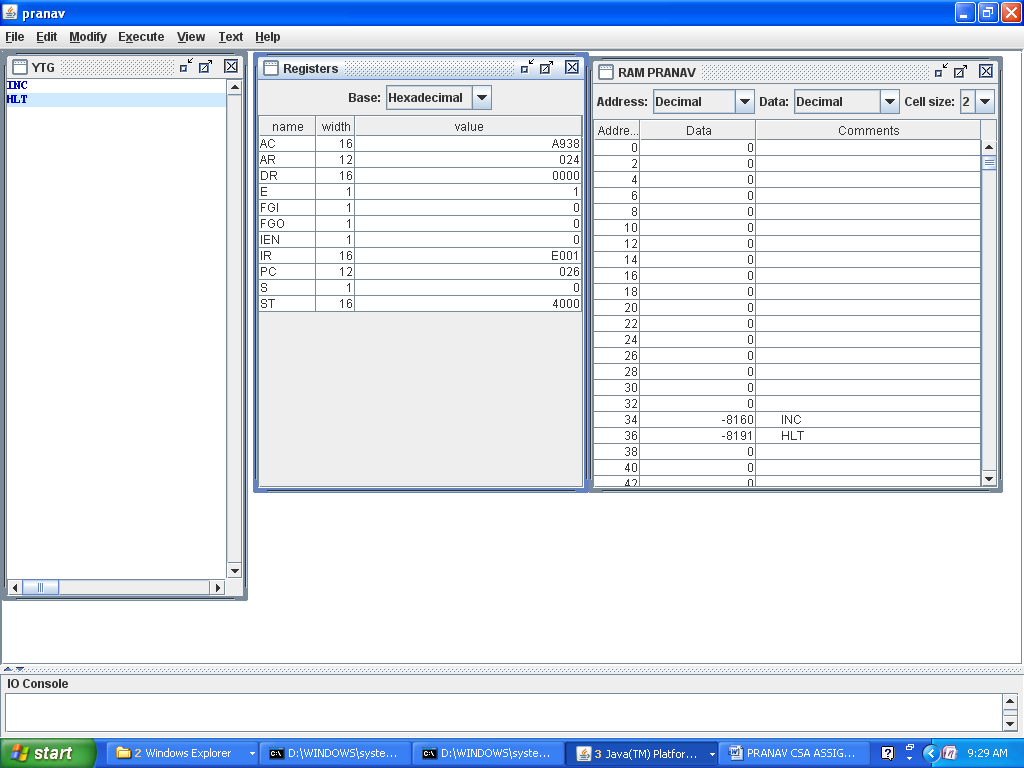
**(SZE**

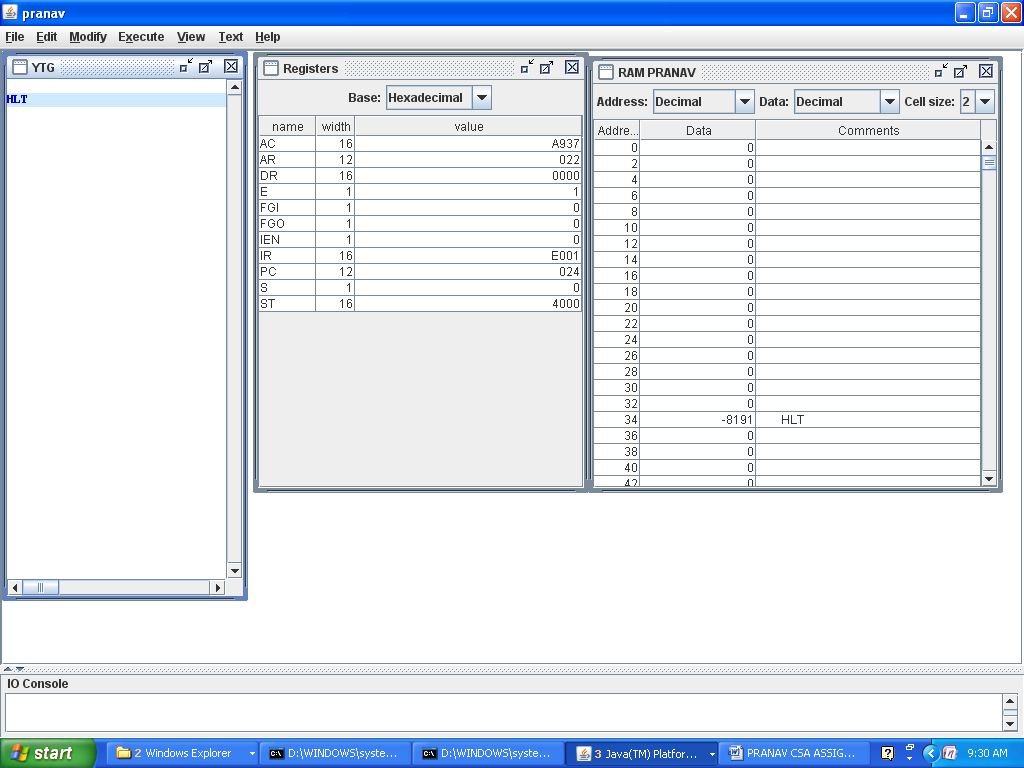
**INC**

**HLT)**

****

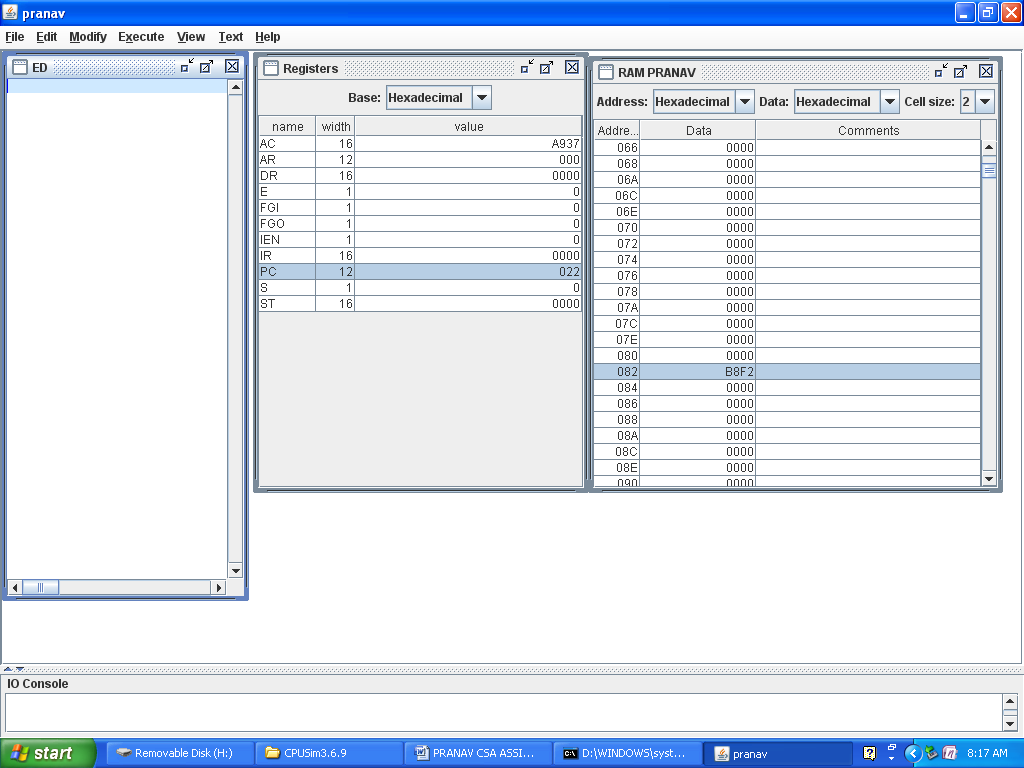
* + 1. **HLT**

****

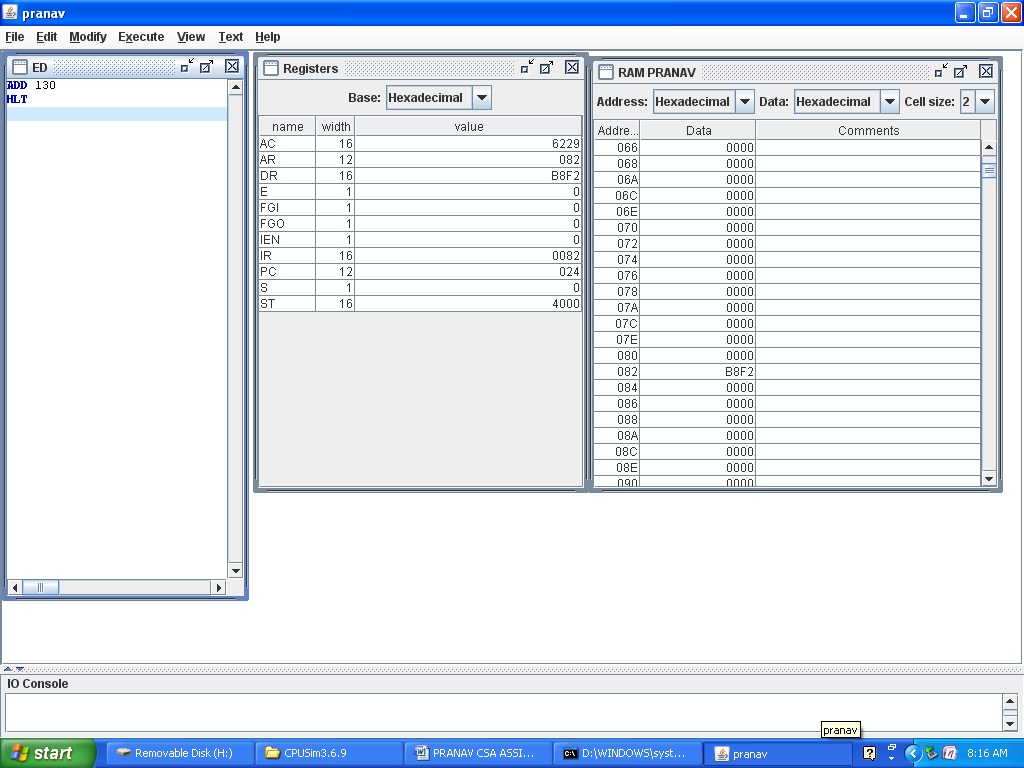
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**QUESTION NO 4**

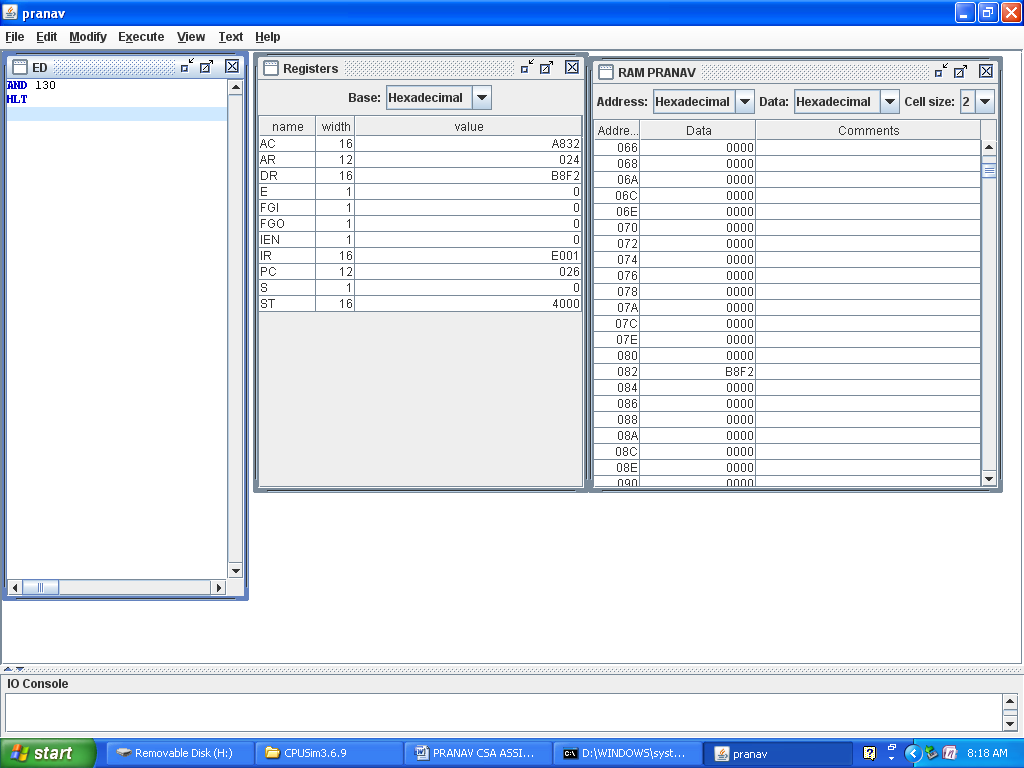
**BEFORE EXECUTION**

****

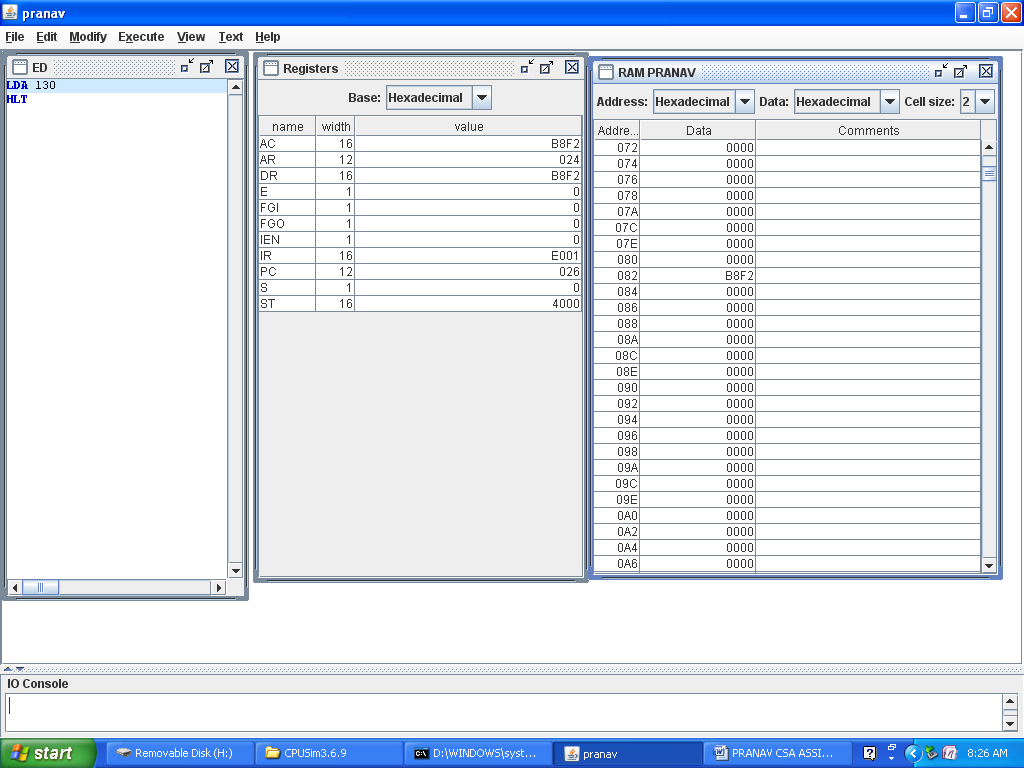
1. **ADD**

****

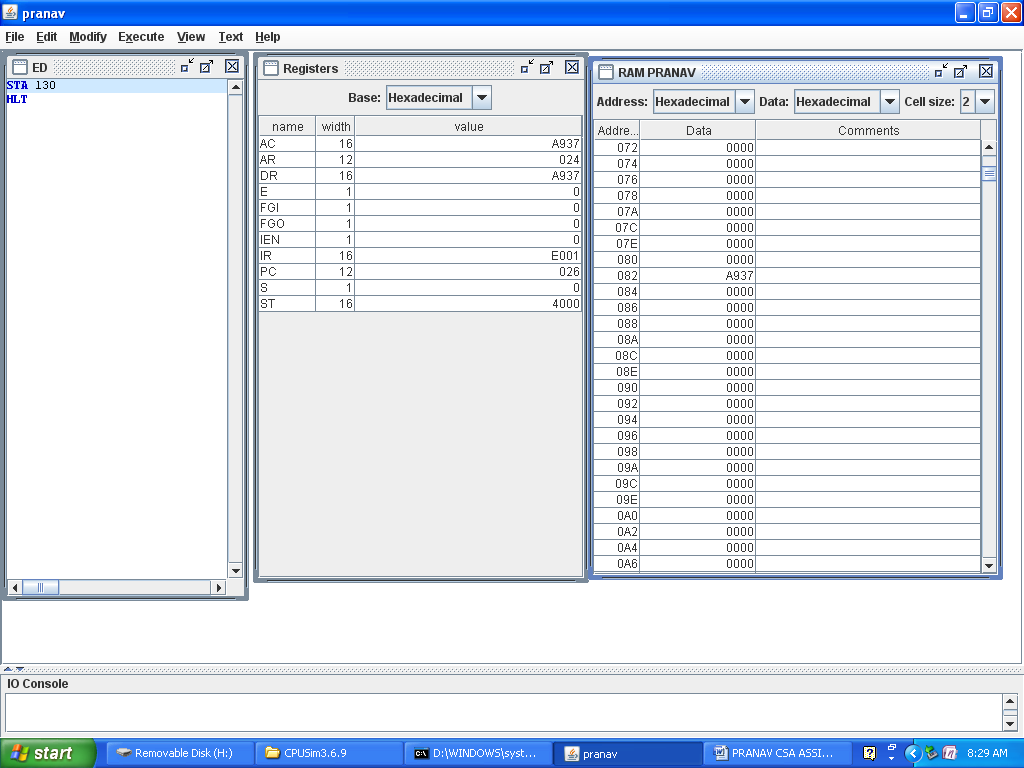
1. **AND**

****

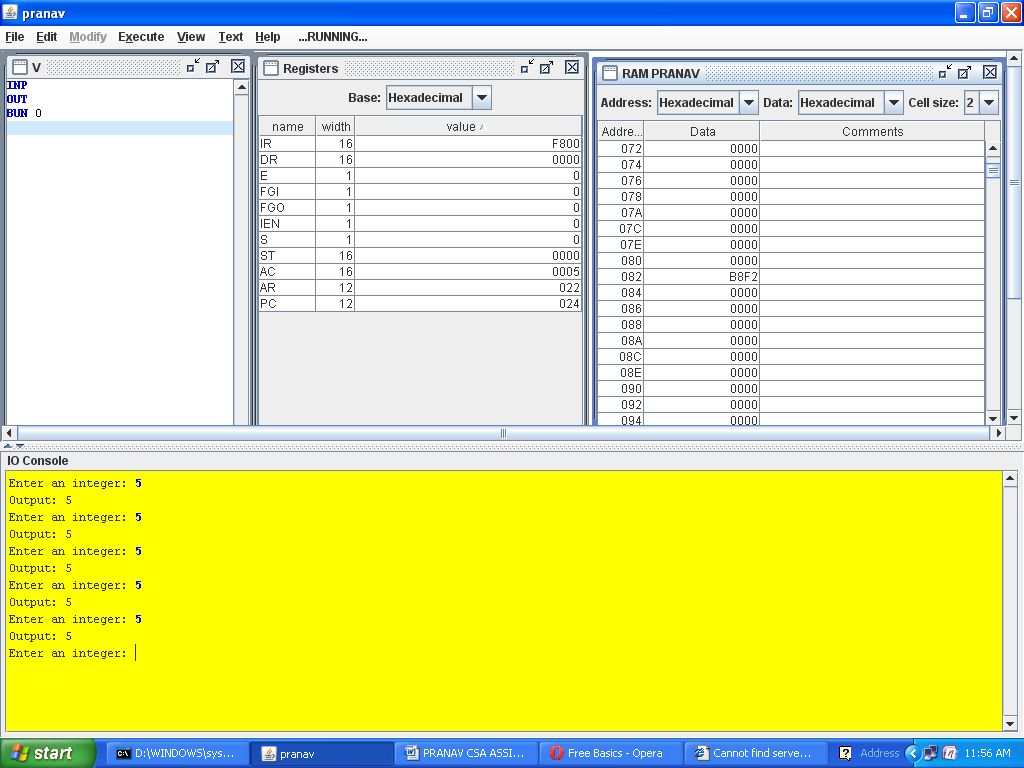
**c.LDA**

****

1. **STA**

****

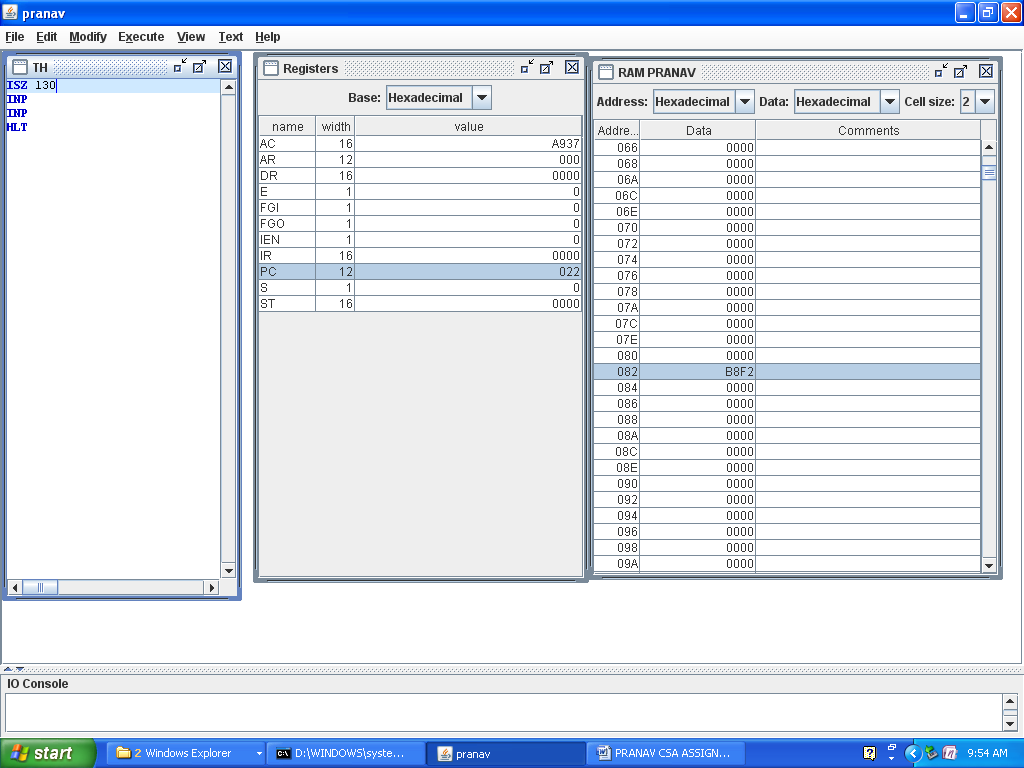
**e.bun**

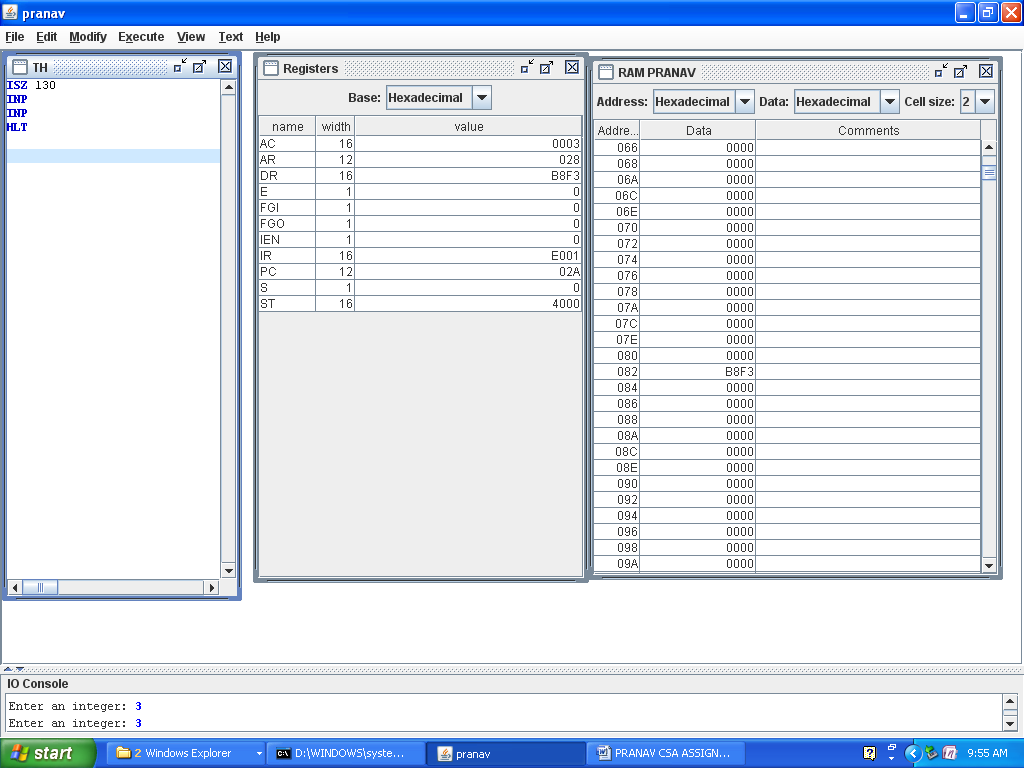
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**f.bsa**

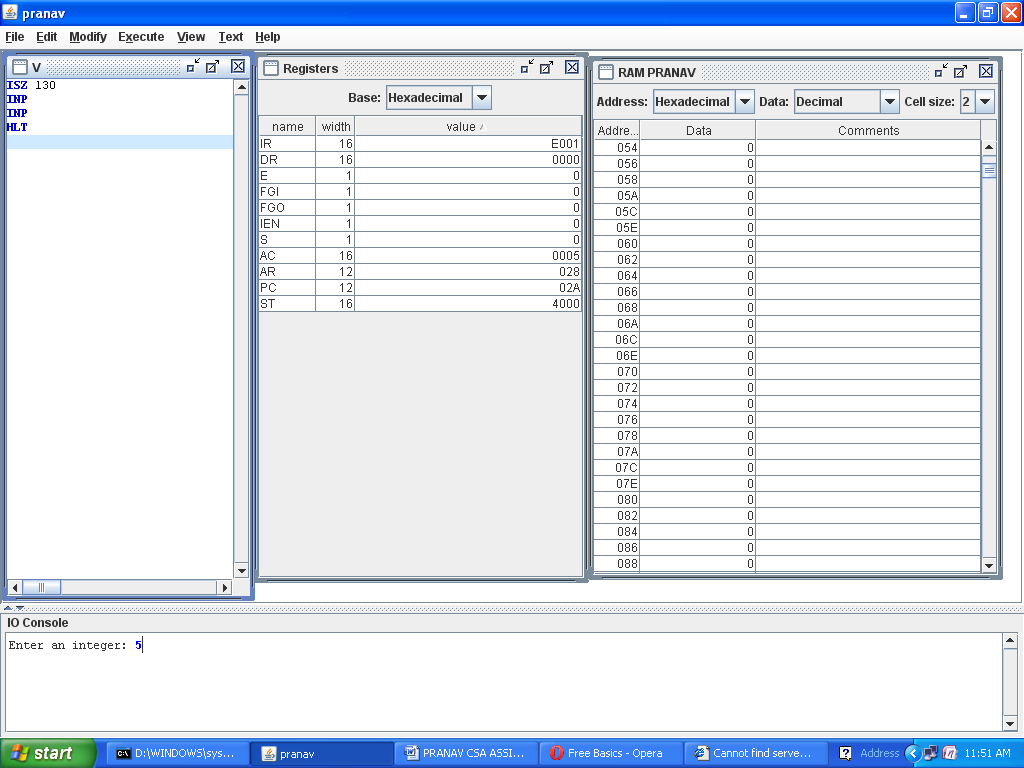
**g.ISZ**

**(BEFORE ISZ)**

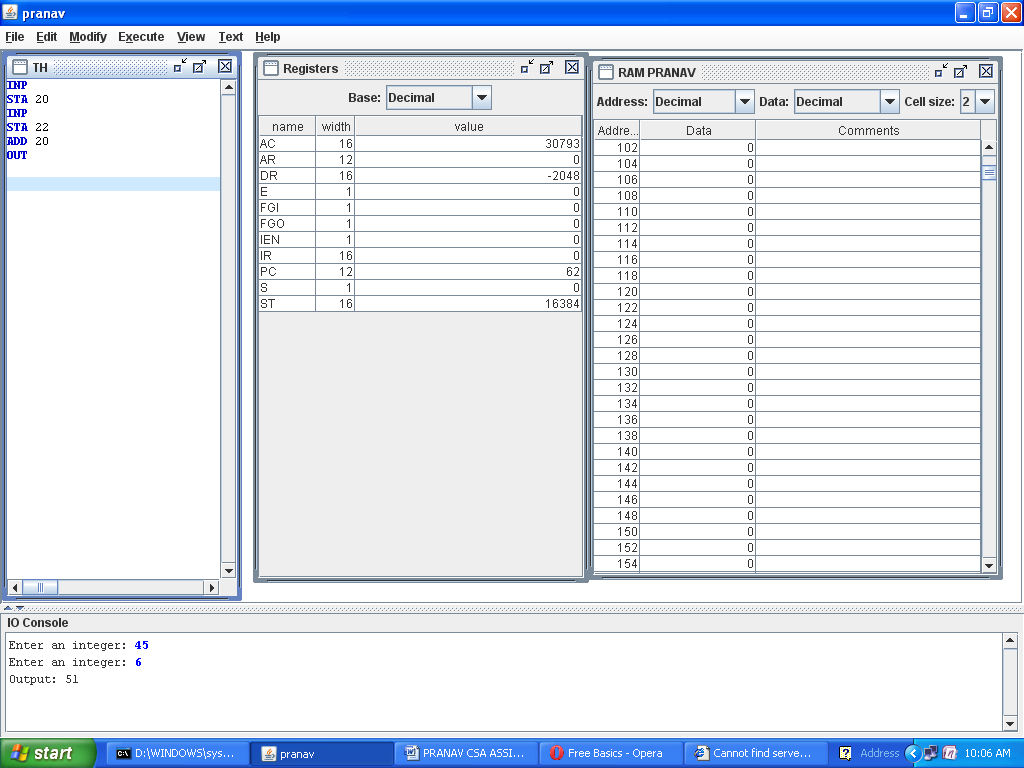
****

****

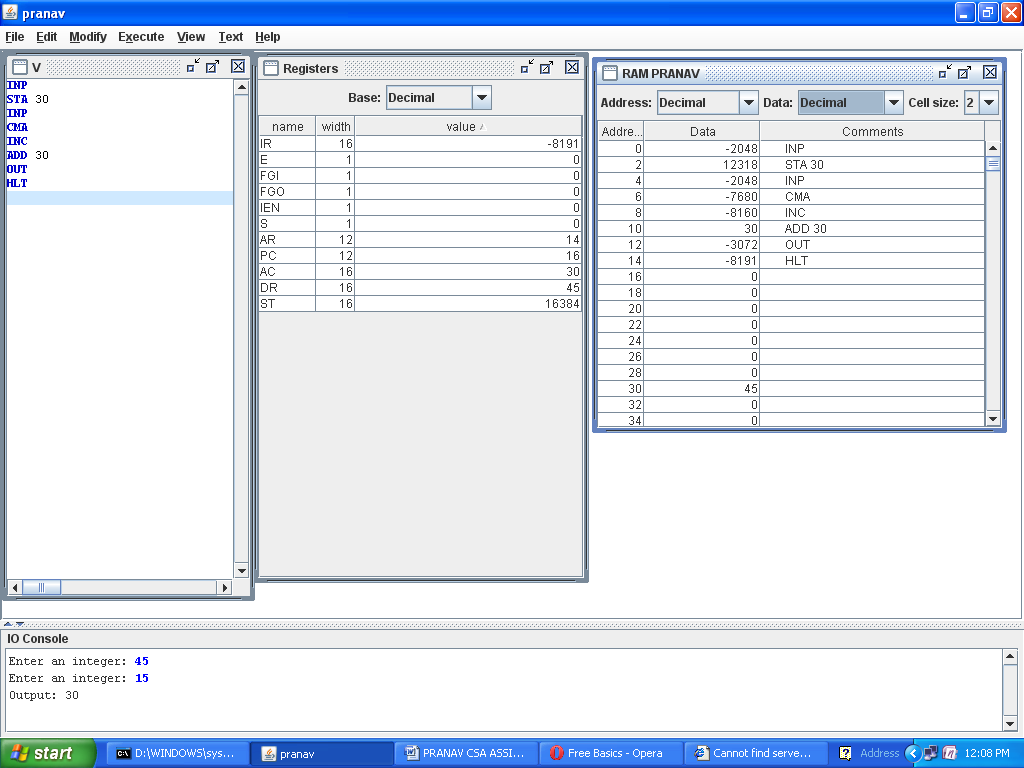
**WHEN DR IS -1**

****

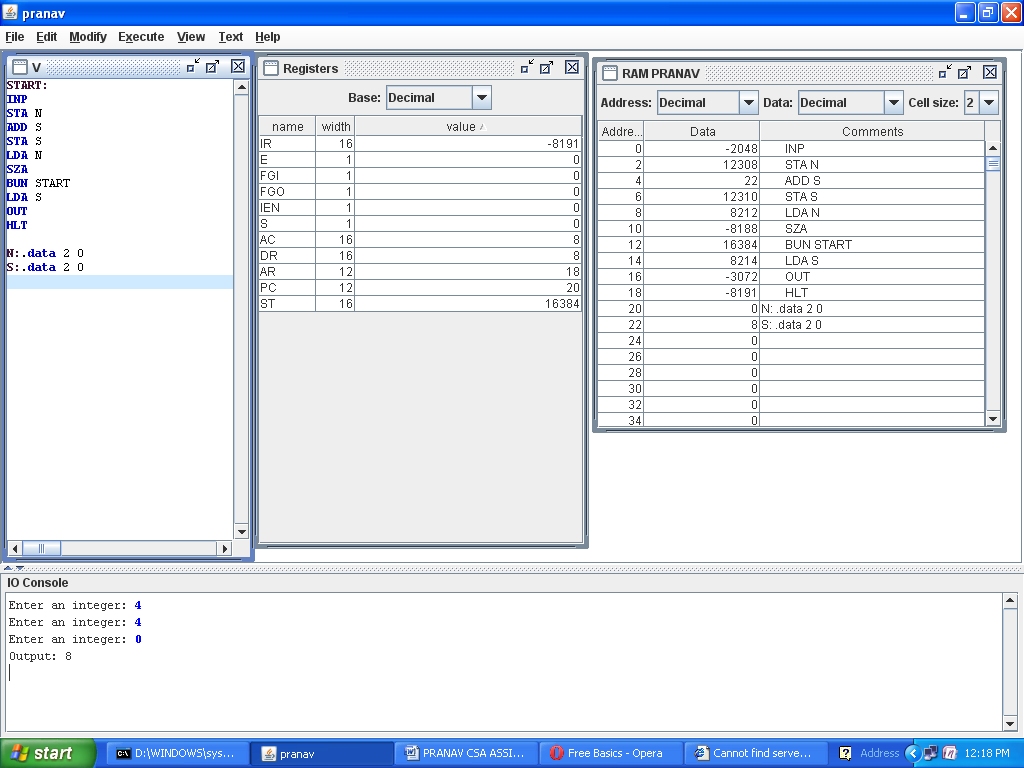
**question 10**

****

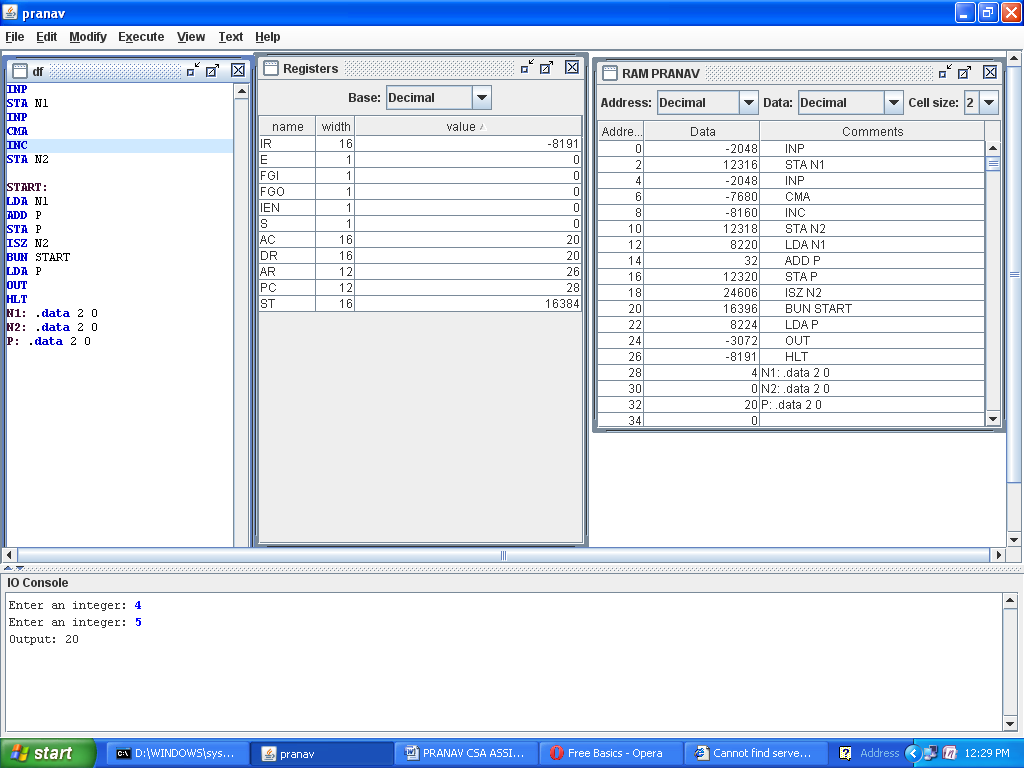
**QUESTION 11 (SUBTRACTION)**

****

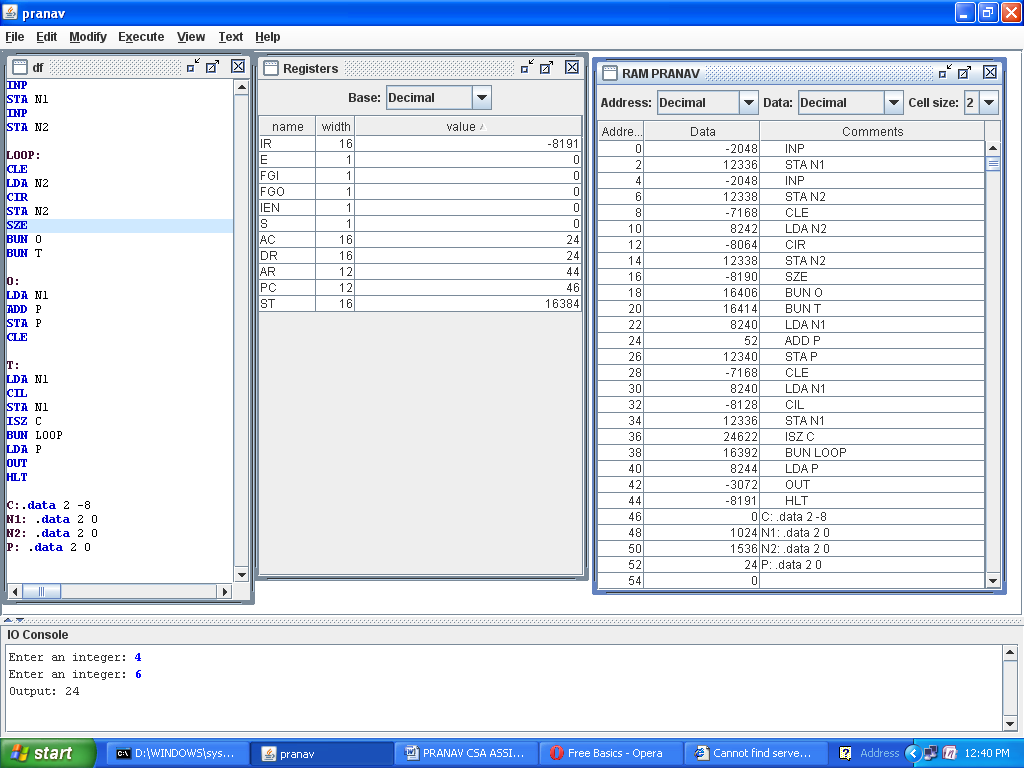
**Ques 12 (Add two no until a zero is entered)**

****

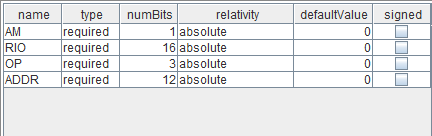
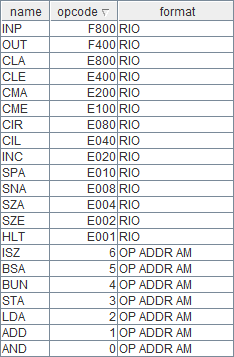
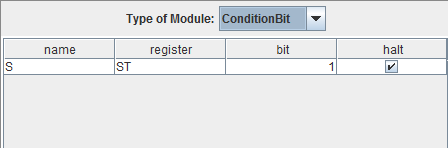
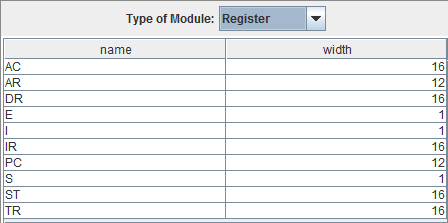
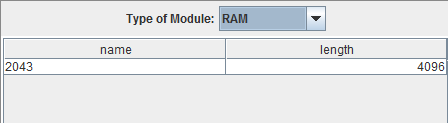
**QUES 13 (MULTIPLY TWO NUMBERS BY SUCCESSIVE ADDITION)**

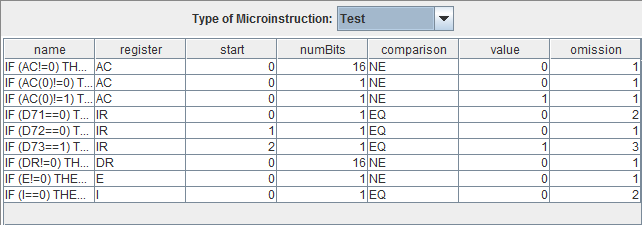
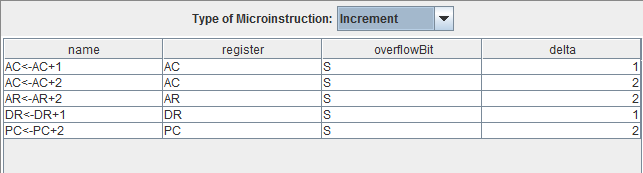
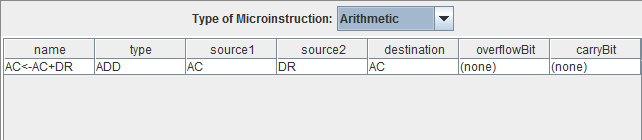
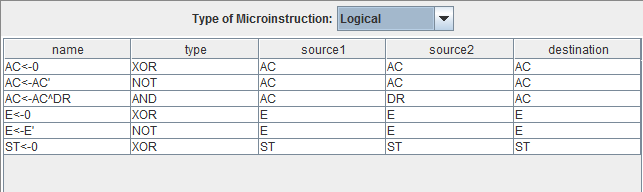
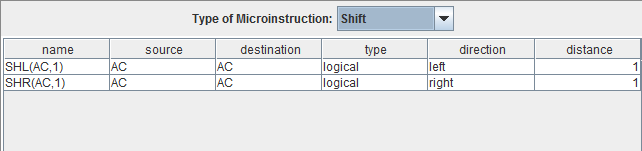
****

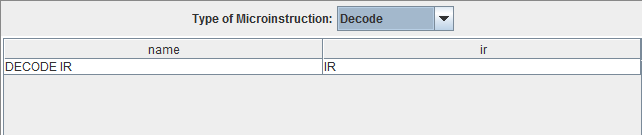
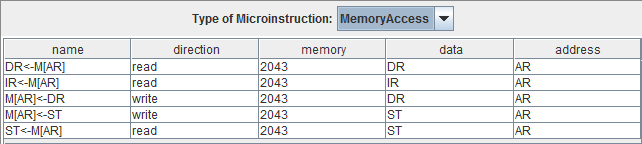
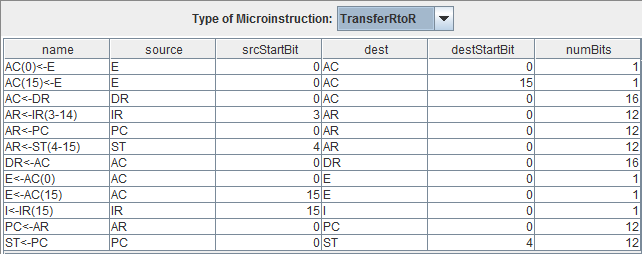
**QUES 14**

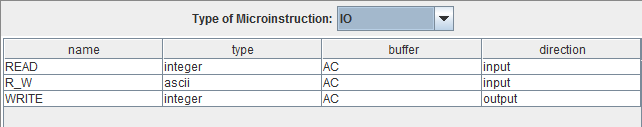
****

**QUES 5 (INDIRECT)**

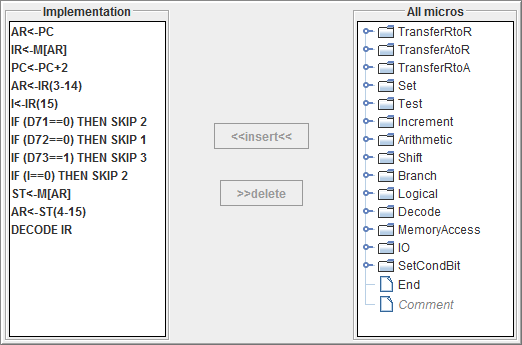
QUESTION 6. LIST OF REGISTERS, RAM OF 4096 BYTES, LIST OF MACHINE INSTRUCTIONS OF INDIRECT MAHINE (WITH I-BIT)

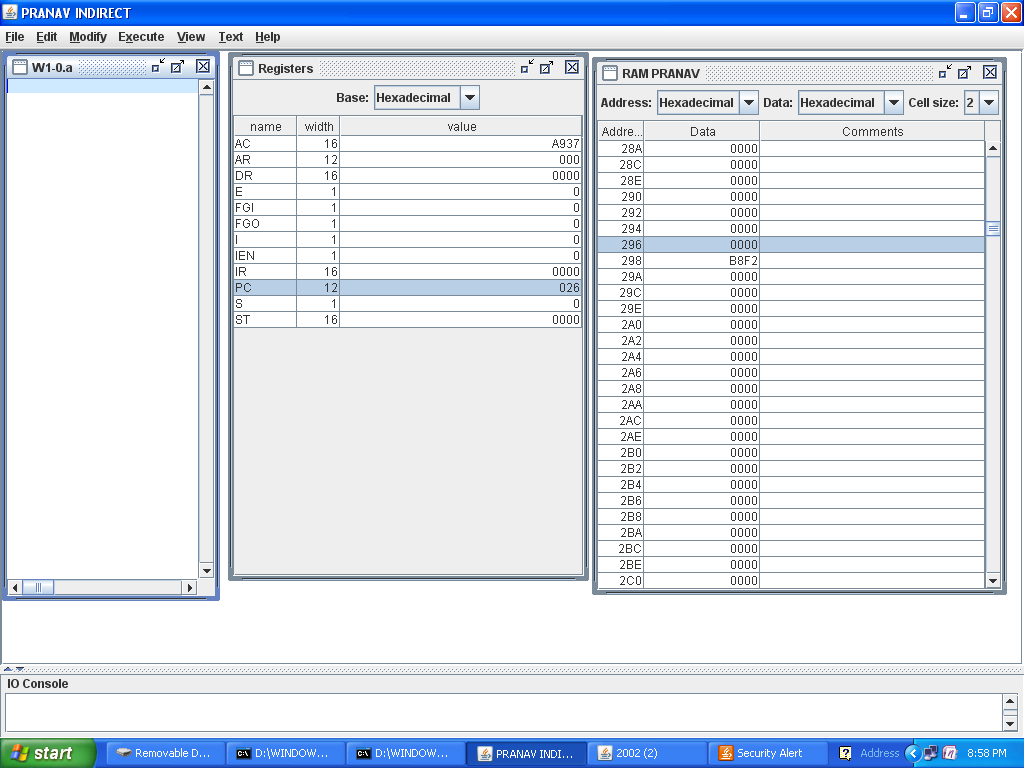
LIST OF MICRO-INSTRUCTIONS



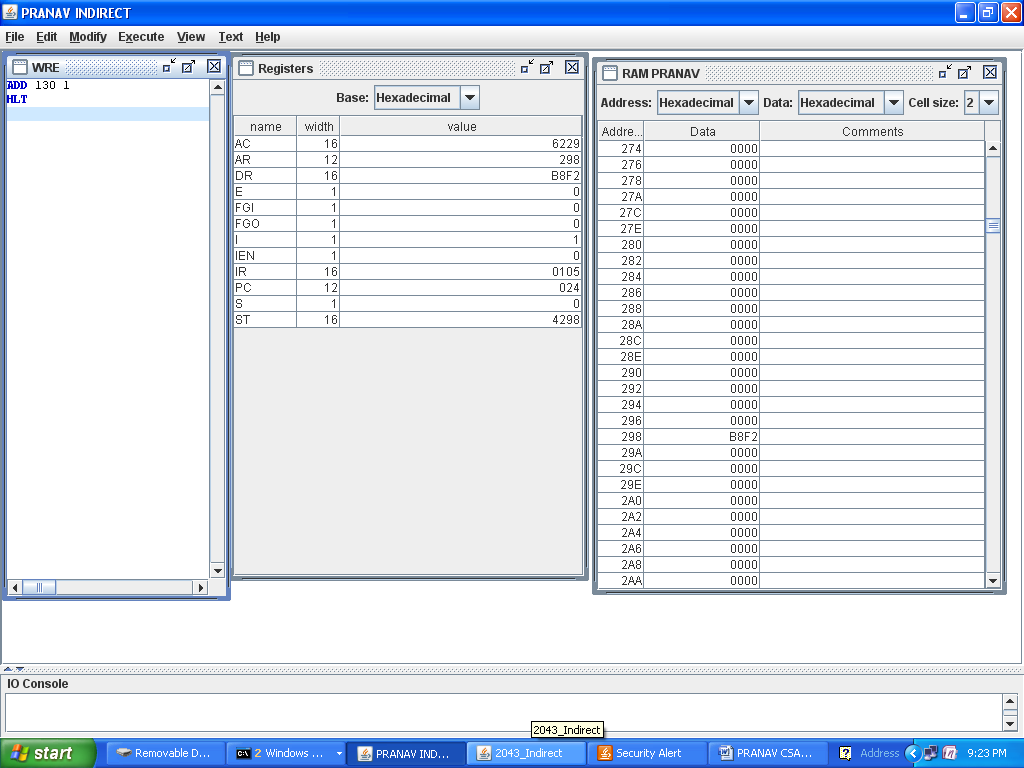


FETCH SEQUENCE FOR INDIRECT MACHINE

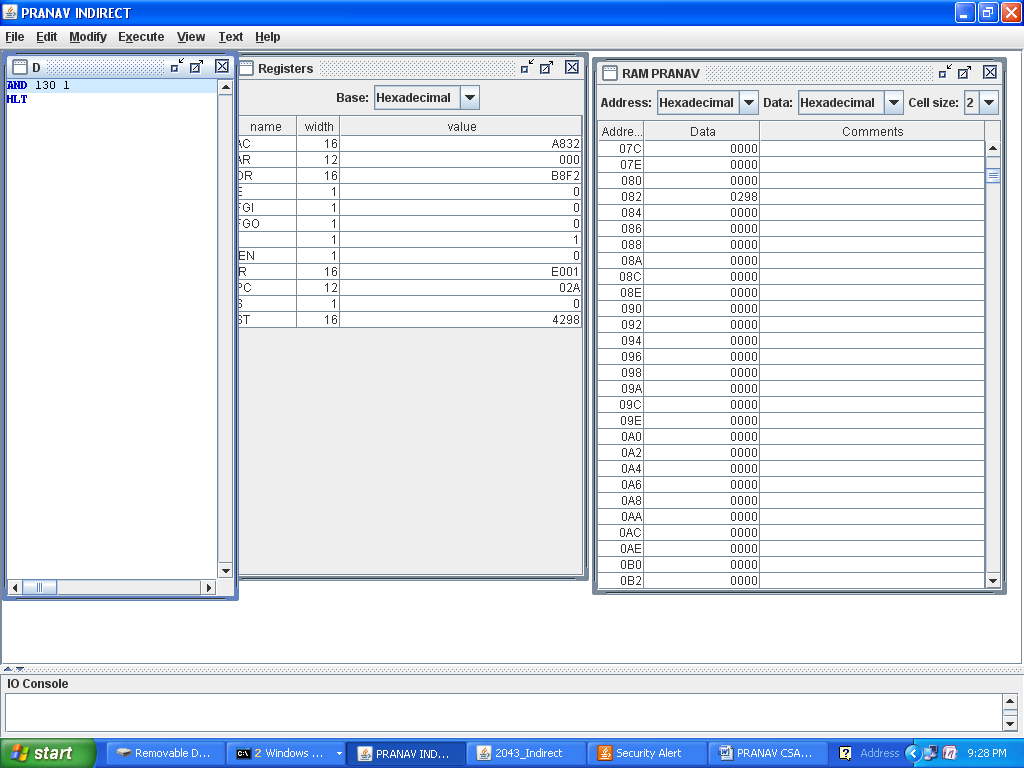


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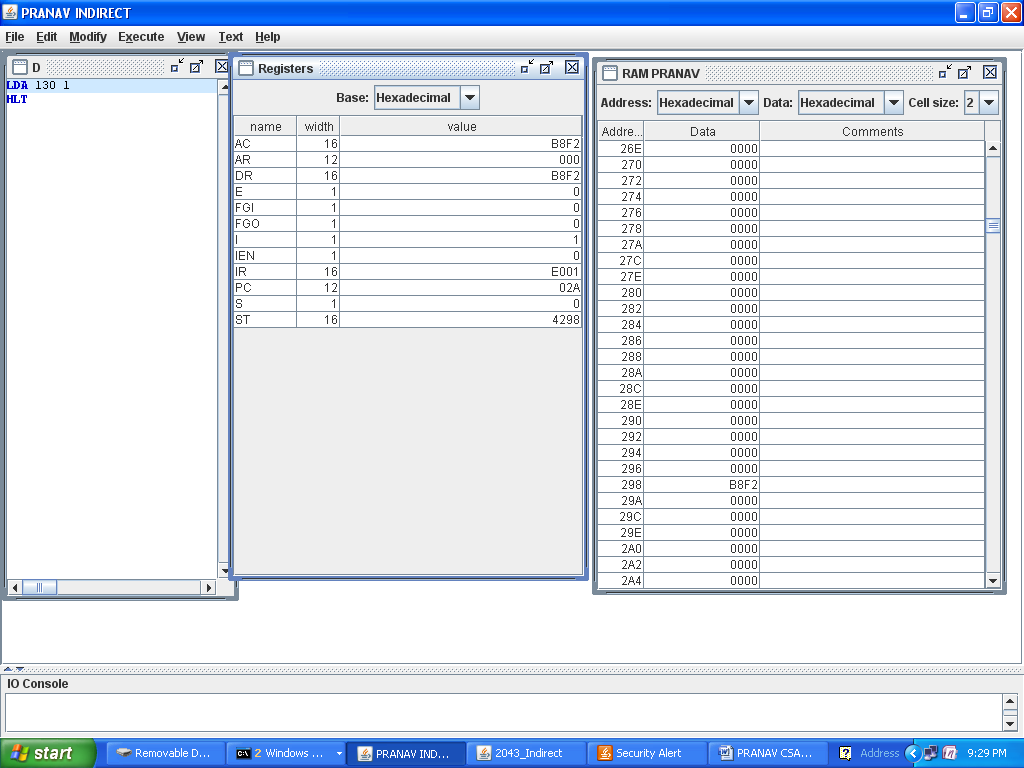
**ADD**

****

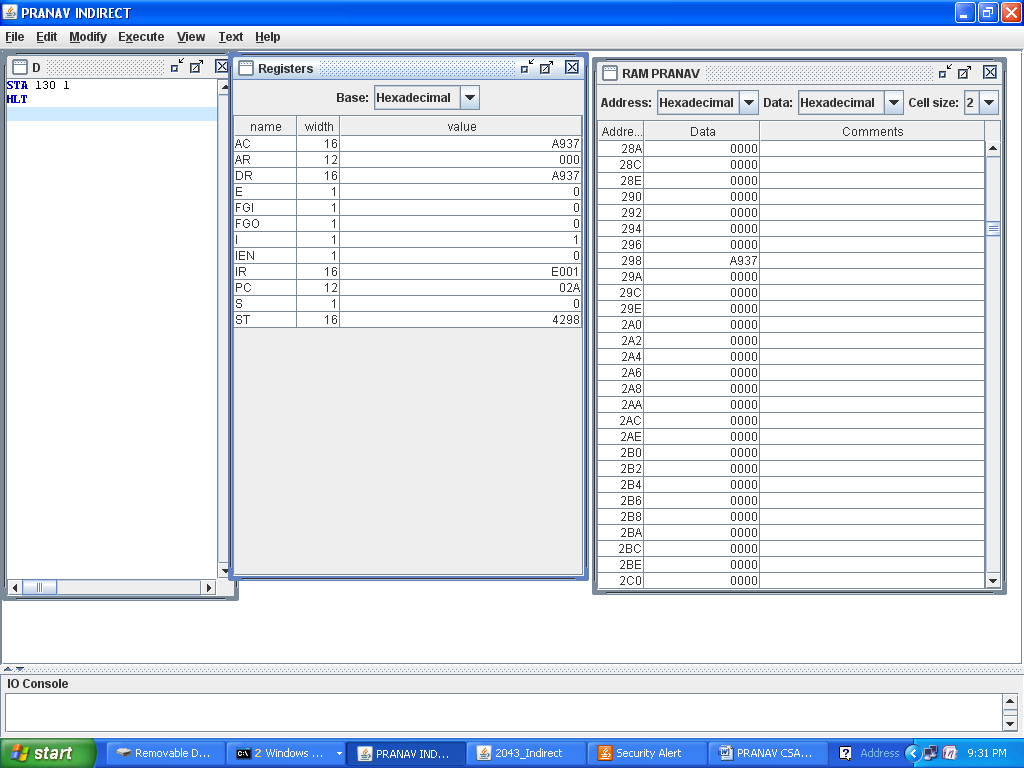
**AND**

****

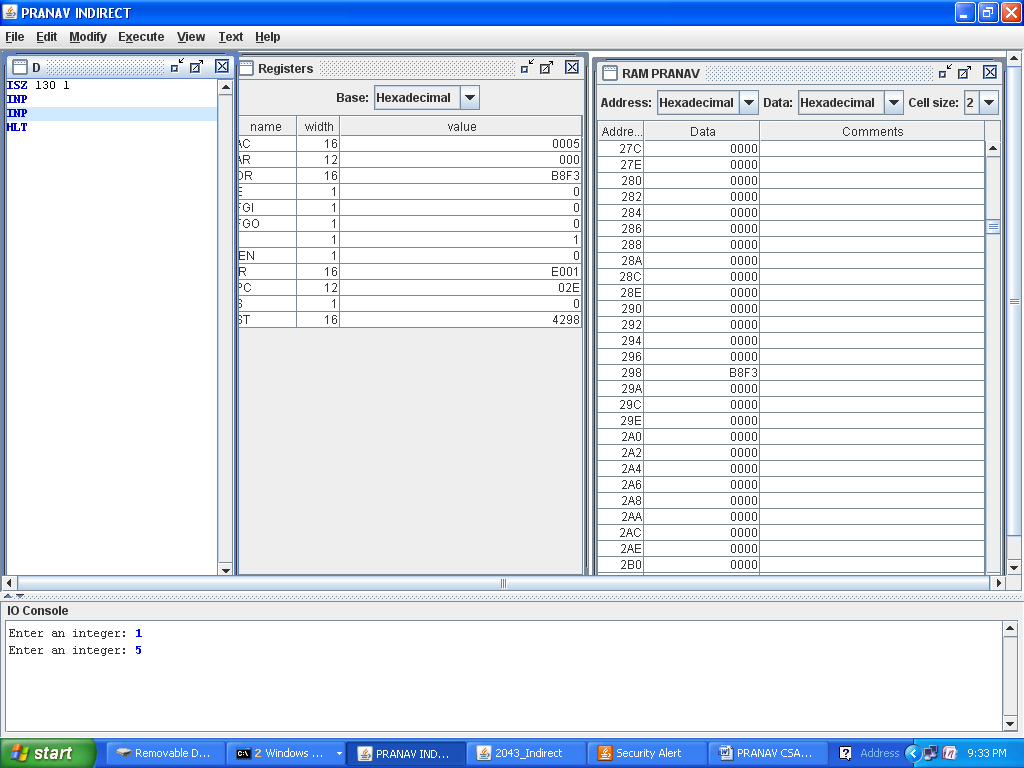
**LDA**

****

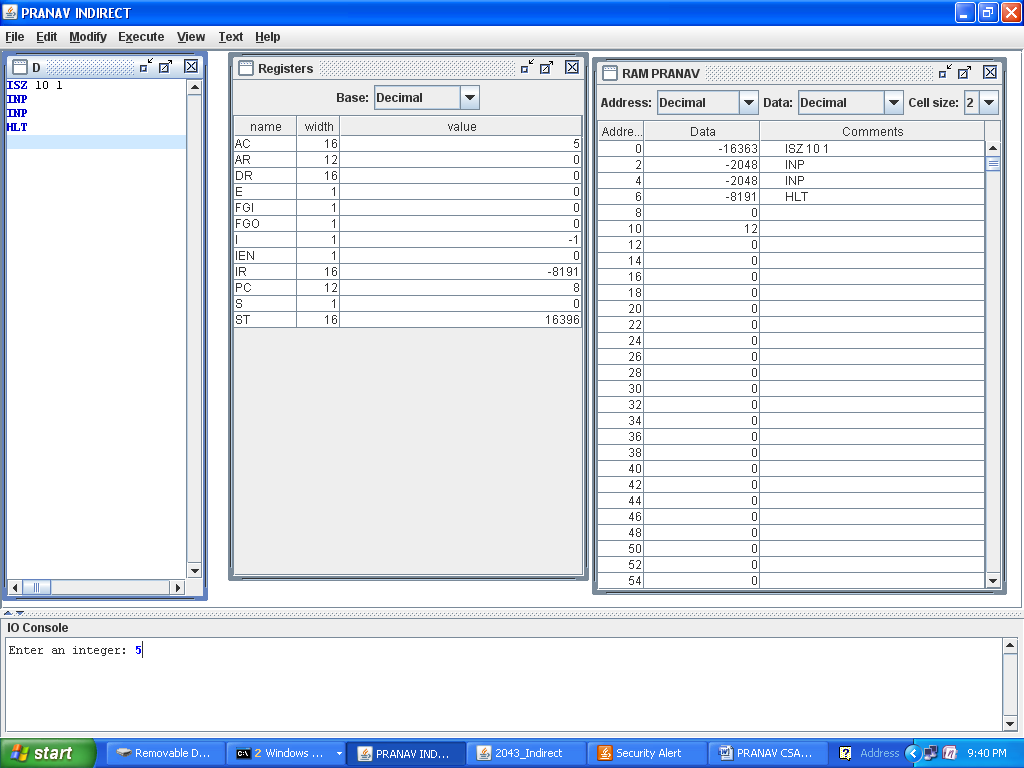
**STA**

****

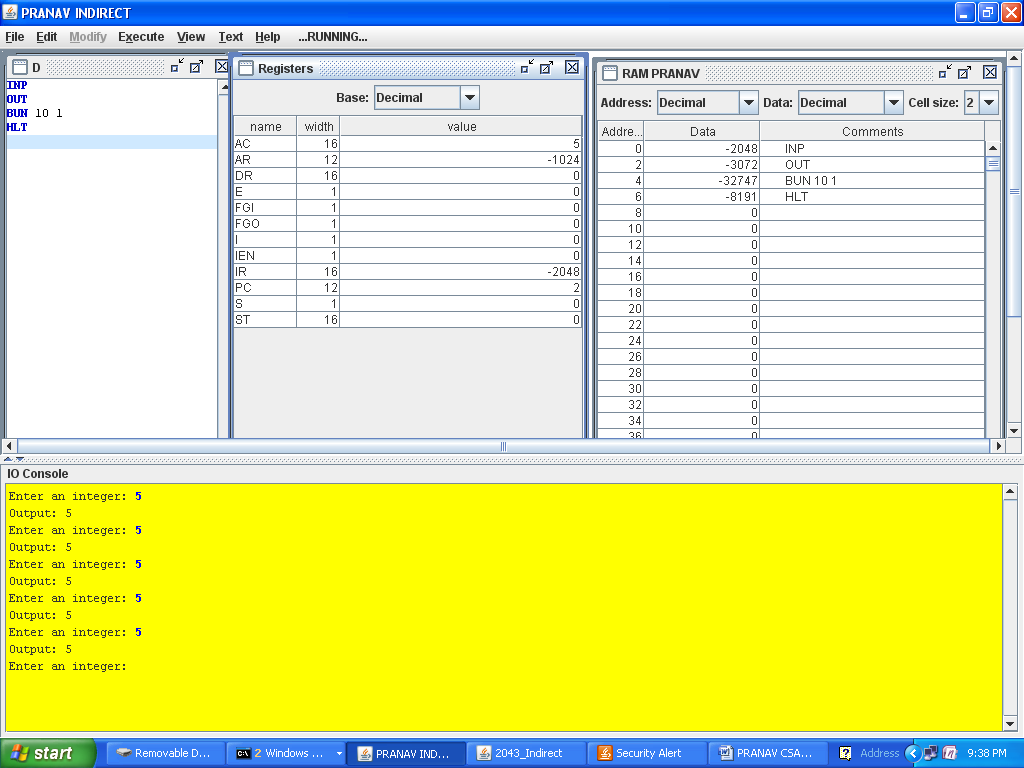
**ISZ**

****

**WHEN DR IS -1.**

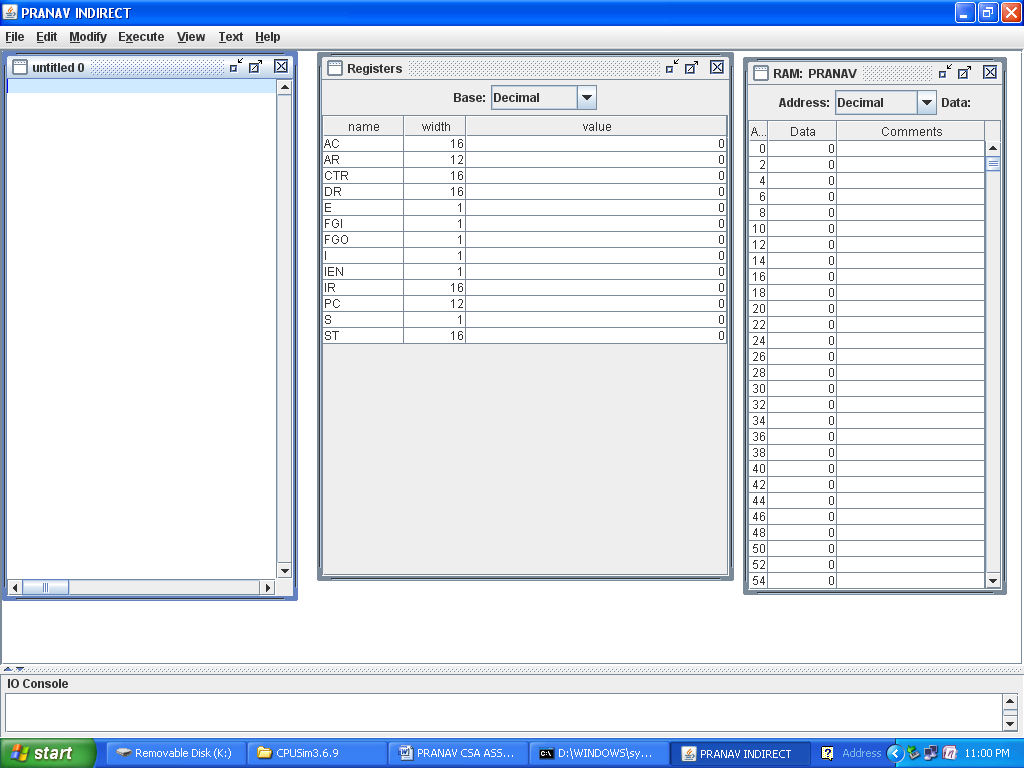
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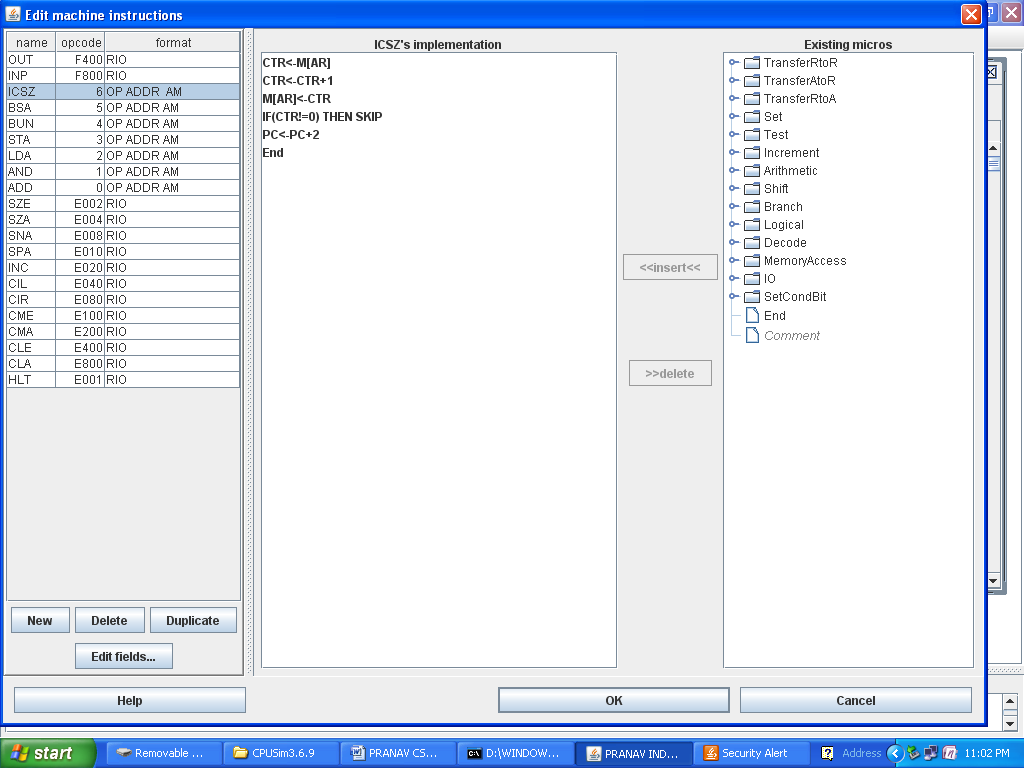
**BUN**

****

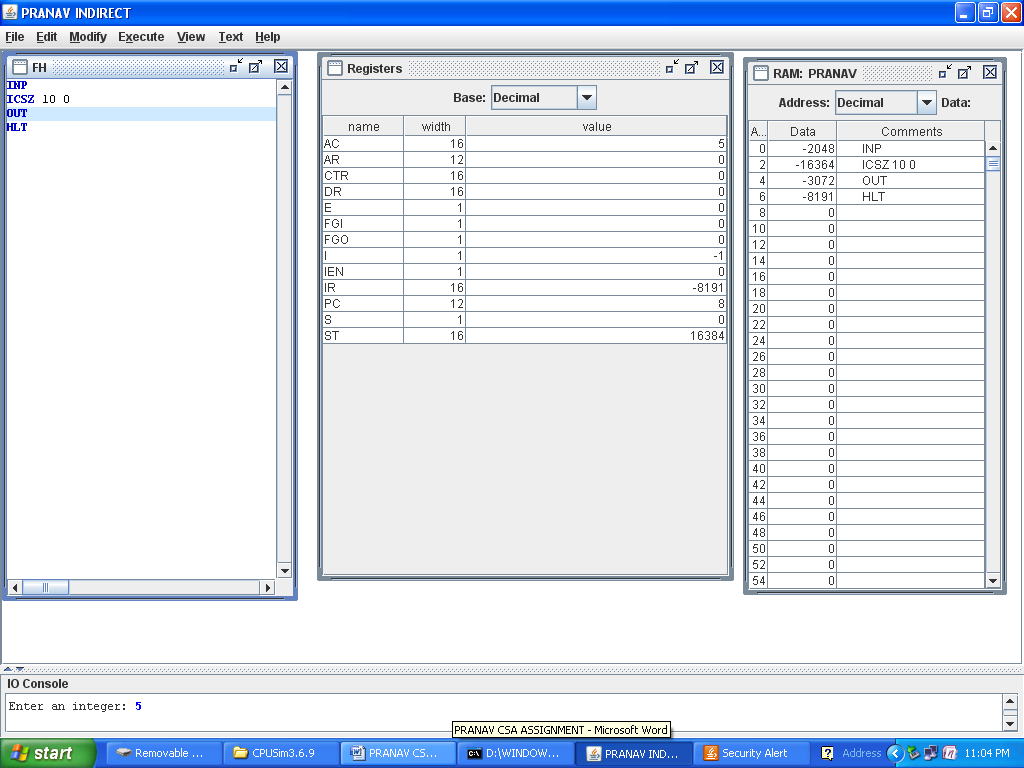
**QUES 9**

**A.REGISTER IS ADDED**

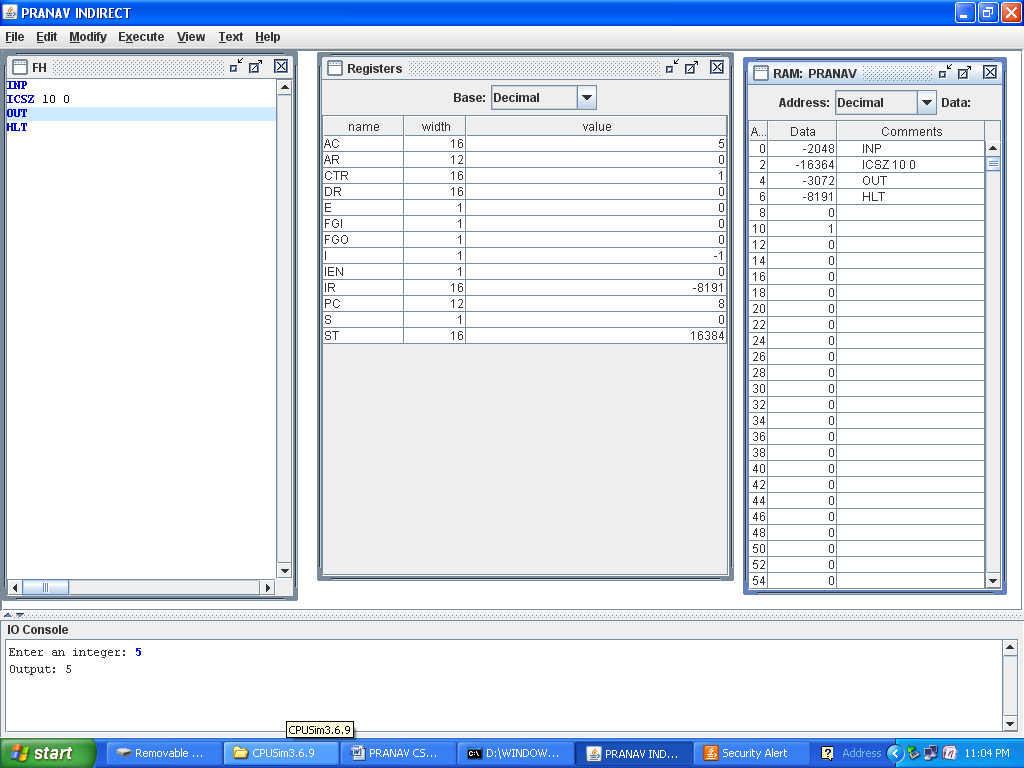
****

****

**WHEN -1 IS PLACED IN CTR**

****

**WHEN ANY OTHER NO PLACED IN CTR**

****